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Fluke

7220A

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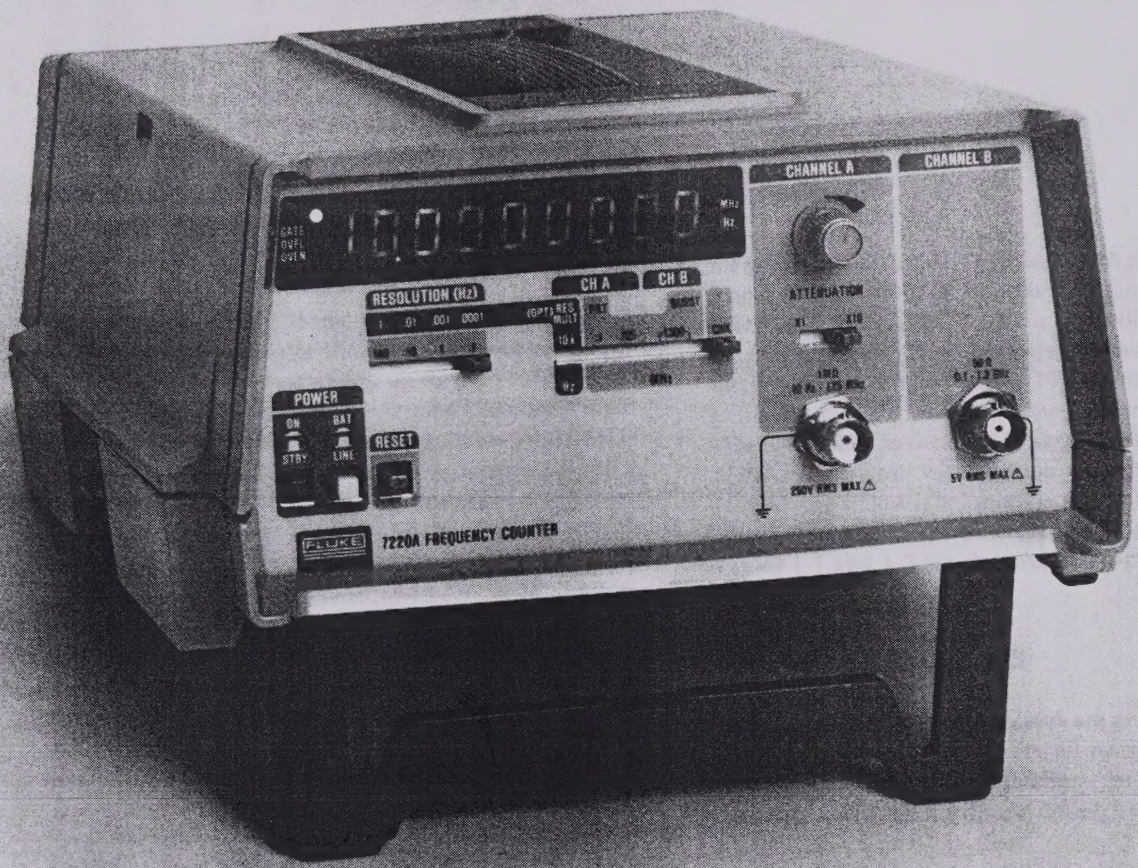


7220A Frequency Counter

Section 1
Introduction & Specifications

1-1. INTRODUCTION

1-2. The John Fluke Model 7220A is a nine-digit portable, bench-type Counter that provides wide-range frequency measurement capability up to 1300 MHz. There are two input channels. The ac-coupled Channel A input allows frequency measurements from 10 Hz to 125 MHz with 1 Megohm input impedance. The Channel B input allows prescaled frequency measurements of continuous wave or burst signals from 100 MHz to 1300 MHz with 50 ohm input impedance. Channel A signal conditioning includes a X10 fixed attenuator and a X10 variable attenuator. For low frequency measurements, a 100 kHz low-pass filter may be selected. Four standard resolution settings and gate times may be selected that allow resolution in decade steps from 100 Hz to 0.1 Hz. Four additional resolution settings (up to .0001 Hz) are available when the Resolution Multiplier Option -351 is installed.

1-3. Measurements are displayed on a nine-digit LED display. Three LED annunciators indicate gate time, measurement overflow, and if optional oven time base is receiving power. The 7220A may be operated with the standard 10 MHz time base, an optional TCXO (Temperature Compensated Crystal Oscillator) time base, or either of two optional low power oven time bases. A self check mode applies the time base signal to the internal counters, thus providing a check for most of the 7220A internal circuitry.

1-4. The 7220A is enclosed in a PTI (Portable Test Instrument) case which includes an inner metal lining for RFI shielding. The counter may be operated at switch selectable line voltages of 100V, 120V, 220V or 240V at 47-63 Hz, or with an optional battery pack.

1-5. OPTIONS AND ACCESSORIES

1-6. When the Battery Pack Option -010 is installed along with one of the optional oven time bases, high measurement accuracy is provided with portable convenience. When the Digital Interface Option -521 is installed in the 7220A, serial BCD data is available at a rear panel output. Option -521 also allows the counter to operate directly into a Fluke 2020A, 2021A, or 2030A Printer (with Option -004 installed in the Printer). When Option -521 is installed in the 7220A, and it is used with a Fluke 1120A Translator with Option -522 installed (in the 1120A), the 7220A is compatible with the IEEE-488 Bus. All of the options are described in detail in Section 6. Tables 1-1 and 1-2 list the available options and accessories for the 7220A.

1-7. SPECIFICATIONS

1-8. Specifications for the 7220A are given in Table 1-3. Comparative specifications for all of the optional time bases are also given. Specifications for the options are included in Section 6 with the option descriptions.

Table 1-1. 7220A Options

OPTION NO.	DESCRIPTION
72XXA-010	Battery Pack
7220A-111	1 PPM TCXO Time Base
72XXA-131	Low Power Oven Time Base
72XXA-132	Superior Low Power Oven Time Base
7220A-351	Resolution Multiplier
72XXA-521	Digital Interface (factory-installed in 7220A)
72XXA-522	Interface PCB Assy (installed in 1120A)
72XXA-529	IEEE-488 Interface (includes Options -521, -522, and Accessory Cable Y7203)

Table 1-2. 7220A Accessories

ACCESSORY NO.	DESCRIPTION	ACCESSORY NO.	DESCRIPTION
A53	Whip Antenna	Y2020	C-Size Panel Adapter
Y2014	C-Size Single Rack Adapter	Y7203	2-Foot Ribbon Cable Assembly
Y2015	C-Size Dual Rack Adapter	Y7204	5-Foot Ribbon Cable Assembly

Table 1-3. Specifications

FUNCTIONS

Frequency A

Range	10 Hz – 125 MHz
Resolution	0.1 Hz, 1 Hz, 10 Hz, 100 Hz
Accuracy	±1 count ± time base errors
Display	MHz with decimal point
Measurement Time	Gate Time* + cycle time**

Frequency B

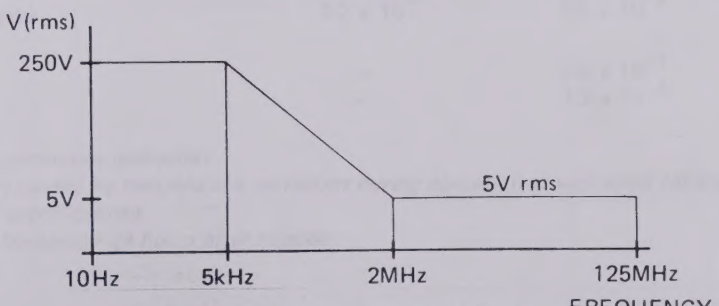
Range	100 MHz – 1300 MHz
Resolution	0.1 Hz, 1 Hz, 10 Hz, 100 Hz
Accuracy	±1 count ± time base errors
Display	MHz with decimal point
Measurement Time	Gate time* + cycle time**
Burst Mode	
Minimum Burst	Gate Time* + 40 ms
Automatic Hold	Display holds last complete reading until Reset

**For gate times, see Table 2-5.*

***Cycle time is approximately 150 ms.*

SIGNAL INPUT – CHANNEL A

Bandwidth	10 Hz – 125 MHz, ac coupled
Sensitivity	10 mV rms at 10 Hz – 50 MHz 15 mV rms at 50 MHz – 100 MHz 25 mV rms at 100 MHz – 125 MHz
Input Impedance	1 Megohm, shunted by 60 pF
Attenuator	X1 to X100, X1 or X10 fixed plus X1 to X10 continuously variable
Filter	100 kHz low pass selectable
Maximum Input Voltage	See chart below:



Channel A Maximum Input Voltage

Table 1-3. Specifications (cont)

SIGNAL INPUT – CHANNEL B

Bandwidth	100 MHz – 1300 MHz
Sensitivity	5 mV rms at 100 MHz to 600 MHz 10 mV rms at 600 MHz to 1000 MHz 40 mV rms at 1000 MHz to 1300 MHz
Input Impedance	50 ohm
VSWR	2.5:1 typical maximum
Maximum Input Voltage	5V rms at 100 MHz to 1300 MHz

SIGNAL INPUT – EXTERNAL TIME BASE

Frequency Required	10 MHz
Sensitivity	300 mV rms
Input Impedance	1 kilohm, shunted by nominal 30 pF, ac coupled
Maximum Input Voltage	3V rms

SIGNAL OUTPUT – TIME BASE

Frequency	10 MHz, square wave
Amplitude	TTL levels
Impedance	200 ohms, nominal

STANDARD TIME BASE

Frequency	10 MHz
Aging Rate per month	$\pm 5 \times 10^{-7}$
Temperature Stability	$\pm 5 \times 10^{-6}$, 0 to 40°C
Line Voltage (± 10% change)	$\pm 1 \times 10^{-7}$
Battery Operation	$\pm 1 \times 10^{-7}$

OPTIONAL TIME BASES

	OPTION -111 1 PPM TCXO	OPTION -131 Low Power Oven	OPTION -132 Superior Low Power Oven
Frequency	10 MHz	10 MHz	10 MHz
Aging Rate			
Per day	–	–	$\pm 3 \times 10^{-9}$*
Per month	$\pm 3 \times 10^{-7}$	$\pm 1 \times 10^{-7}$*	$\pm 5 \times 10^{-8}$*
Per year	$\pm 1 \times 10^{-6}$	–	–
Accuracy with temperature** (0° to 40°C)	$\pm 1 \times 10^{-6}$	$\pm 1 \times 10^{-7}$	$\pm 3 \times 10^{-8}$
Line Voltage	$\pm 2 \times 10^{-7}$	$\pm 2 \times 10^{-8}$	$\pm 4 \times 10^{-9}$
Battery Operation	$\pm 2 \times 10^{-7}$	$\pm 5 \times 10^{-8}$	$\pm 1 \times 10^{-8}$
Warm up***			
10 Min	–	$\pm 5 \times 10^{-7}$	$\pm 5 \times 10^{-7}$
20 Min	–	$\pm 3 \times 10^{-8}$	$\pm 3 \times 10^{-8}$

**After 5 days continuous operation.*

***Includes errors caused by temperature variations during operation as well as all calibration errors when calibrated per specifications.*

****Compared to frequency 24 hours after turn-on.*

Table 1-3. Specifications (cont)

GENERAL

Display Annunciation	9-digit LED, with leading zero suppression and decimal point. Three LED annunciators: Gate, Measurement Overflow, Oven Time Base Power
Cycle Rate	In continuous measurement mode, time between end of one gate time and beginning of next gate time is fixed at approximately 150 ms.
Self Check	Counts and displays 10 MHz Time Base.
Reset	Reset switch clears display; holding Reset lights all 9-digit LED segments, releasing Reset allows new measurement to take place.
Power Requirements	24 VA maximum
Line Voltage	100V, 120V, 220V or 240V ac ± 10%, internally selectable
Line Frequency	47–63 Hz
Dimensions	40.3 cm L x 20.3 cm W x 10.8 cm H (12.9 in L x 8.0 in W x 4.3 in H) See Figure 1-1.
Operating Temperature	0° to 40°C
Storage Temperature	-40° to 70°C
Weight	3.2 kg (7 lbs)
EMI	Internal metal RFI shield meets most requirements of MIL-STD-461, notice 3.
Protection Class 1	Relates solely to insulation or grounding properties defined in IEC 348.

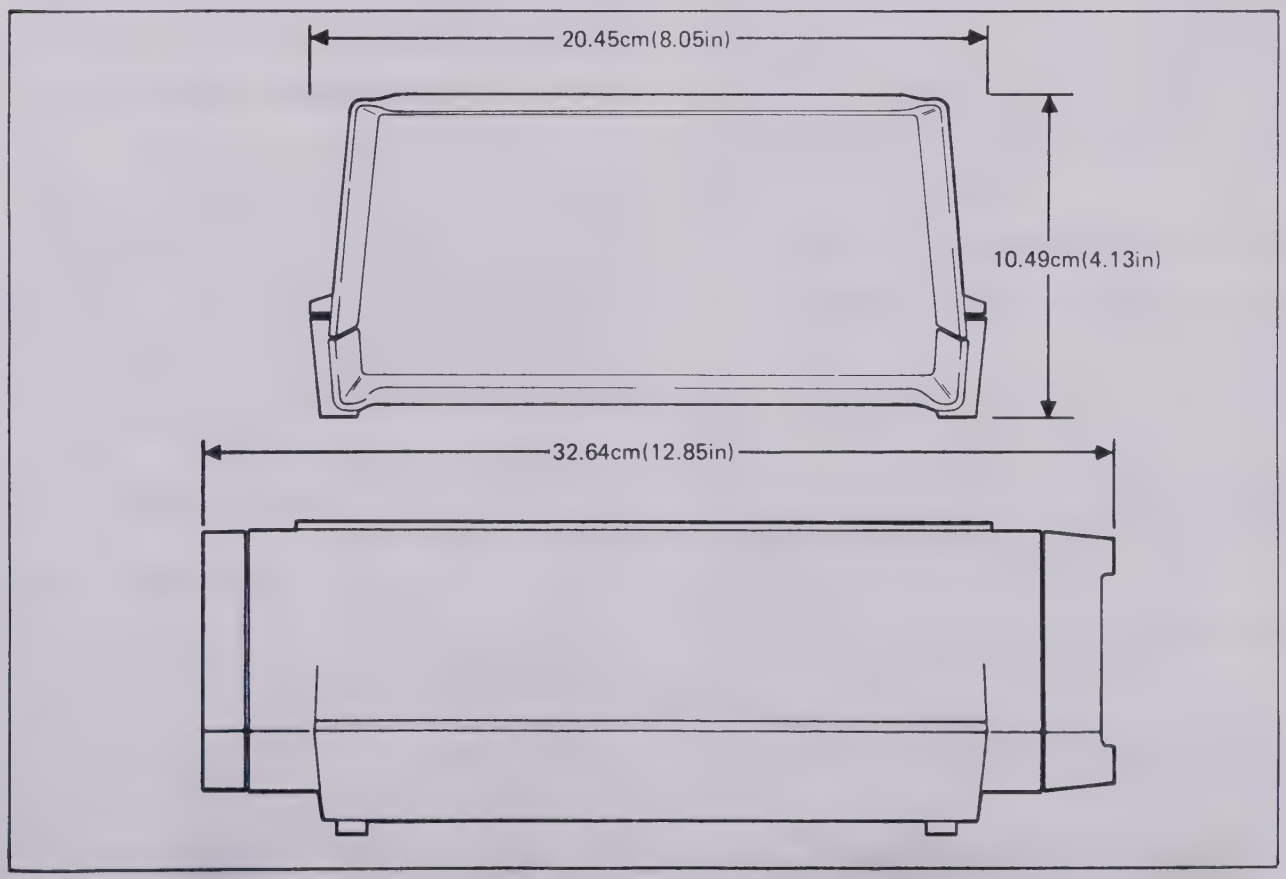


Figure 1-1. Outline Drawing

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. This section of the manual contains information concerning the installation and operation of the Model 7220A Frequency Counter. The contents of this section should be read before operating the counter. Should any difficulties arise during operation of the instrument, please contact your nearest John Fluke Sales Representative, or the John Fluke Mfg. Co., Inc. (P.O. Box 43210, Mountlake Terrace, WA., 98043; Telephone 206 774-2211). A list of sales representatives is given in Section 7.

2-3. SHIPPING INFORMATION

2-4. The 7220A is packaged and shipped in a foam-packed container. Upon receipt of the instrument, make a thorough inspection for proper contents and possible shipping damage. Special instructions for inspection and claims are included with the shipping container. If reshipment is necessary, use the original container. If the original container is not available, a new container can be obtained from the John Fluke Mfg. Co., Inc. Please specify the instrument model number when requesting a new shipping container.

2-5. INSTALLATION

2-6. Input Power

2-7. The 7220A can be operated with an input line voltage of 100, 120, 220, or 240V ac (±10%). Line frequency may vary between 47 and 63 Hz. A rear panel decal specifies the voltage selected prior to shipment. If a change in voltage is required, have a qualified technician perform the procedure. The selection procedure is given in Section 4 of this manual. Replace the fuse when the line voltage setting is changed. Proper fuse ratings are given under Fuse Replacement.

2-8. Fuse Replacement

2-9. The ac input line and the Channel B input line are both fuse protected. The ac input line fuse (F1) is accessible by way of a rear panel fuse holder located to the right of the input power connector. If fuse replacement is required, disconnect the 7220A from line power and remove the fuse cap and fuse (twist the fuse cap ccw using a screwdriver). Select and install a replacement fuse with a rating that is compatible with the local line voltage. Replacement fuse information for the line power fuse is available on the rear panel decal and in the following list. Channel B fuse replacement requires removal of the instrument covers, and should only be performed by a qualified technician. The Channel B fuse replacement procedure is given in Section 4.

1. 100 to 120V ac use fuse type MDL slo-blo 1/4A

2. 220 to 240V ac use fuse type MDL slo-blo 1/8A

2-10. Stacking PTI Instruments

2-11. The stacking feature of the PTI case allows the 7220A to be stacked with, and locked to other Fluke instruments in the PTI product line. Use the following procedure to stack PTI instruments:

1. Locate and pull the black latches on both sides of the unit to their extended position.

2. Place the unit on top of the PTI stack with the front panel toward the front of the stack. See Figure 2-1.

3. When the unit is properly seated, push both latches in. This will lock the unit to the stack.

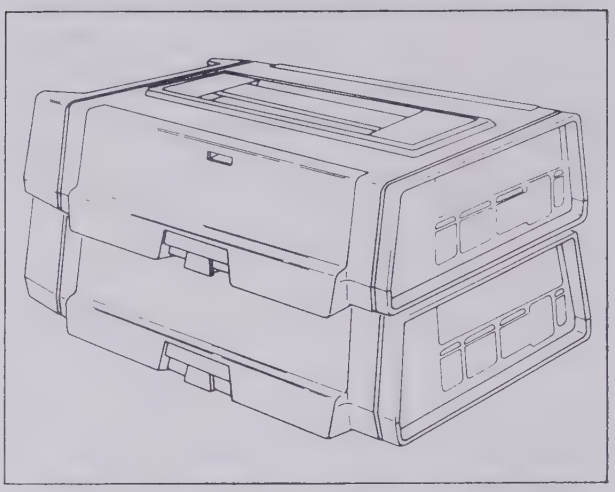


Figure 2-1. Stacking PTI Instruments

2-12. Tilt-Down Bail

2-13. When used as a separate instrument, the 7220A may be tilted up, or down, with the aid of the tilt bail. In the extended position, the bail may be locked in place by firmly pressing the legs into slots provided in the bottom panel. When retracted, the bail lies flush with the bottom panel and does not interfere with case stacking. The bail is normally mounted toward the front of the instrument. To remove the bail, compress either of its legs toward the center of the case and pull out. Installation may then be made in identical mounts at the rear of the bottom panel.

2-14. Rack Installation

2-15. The 7220A may be installed in a standard 19-inch equipment rack or a DIN panel mount. Mounting kits for these accessories are described in Section 6 of this manual. A list of all available accessories and options is presented in Section 1.

2-16. OPERATING FEATURES

2-17. The function and location of all 7220A controls, indicators, and connectors are shown in Figures 2-2 and 2-3, and described in Tables 2-1 and 2-2.

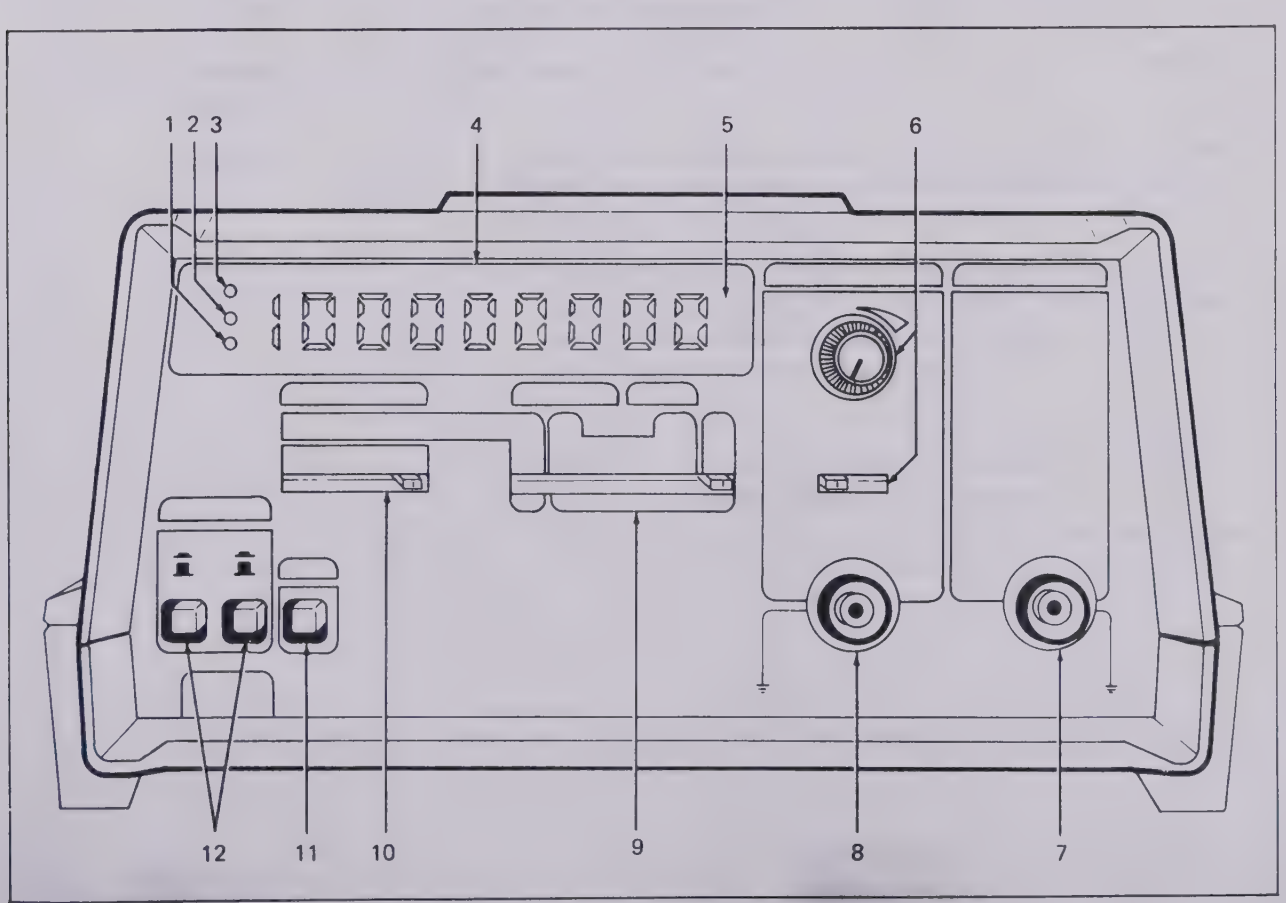


Figure 2-2. 7220A Front Panel Controls, Indicators and Connectors

Table 2-1. 7220A Front Panel Controls, Indicators, and Connectors

REF. NO.	NAME	FUNCTION
1	OVEN Annunciator	Illuminates if an oven time base is installed and is receiving power
2	OVFL Annunciator	Illuminates if the accumulator has exceeded the measurement range selected.
3	GATE Annunciator	Illuminates while the Main Gate is enabled and the input frequency is being counted.
4	Display	A nine digit LED measurement display with automatic decimal point placement and leading zero suppression.
5	Measurement Units Indicator	Indicates the units for the measurement displayed. All measurements are displayed in MHz, except when the Resolution Multiplier Option is selected using the Function Control. Then the measurement is displayed in Hz.
6	ATTENUATION Controls	These two controls (which only affect Channel A) can be used to limit the input signal to the dynamic operating range of the input amplifier. The upper rotating control allows variable attenuation between X1 and X10. The lower two-position slide switch allows step attenuation of X10. The two controls can be used separately or together to allow total attenuation range of X1 to X100.
7	CHANNEL B Connector	BNC input connector for Channel B. Channel B has a 50 ohm input impedance and is internal fuse protected.
8	CHANNEL A Connector	BNC connector for Channel A. Channel A has a 1 megohm input impedance.
9	CH A/CH B	A six-position slide switch which allows selection of 7220A operating mode. Moving the slide between positions automatically generates a Reset command for the instrument. The function of each operating mode is as follows: CHK Initiates instrument self-test. The 10 MHz time base signal from the instrument is applied to the counting circuitry. This allows an internal check of all instrument circuits except the input circuits. In this mode, the frequency displayed should be 10 MHz. CH B 1300 Enables Channel B measurement of signals from 100 MHz to 1.3 GHz (1300 MHz). 1300 BURST Enables measurement of burst signals from 100 MHz to 1.3 GHz (1300 MHz). CH A 125 Enables Channel A measurement of signals from 10 Hz to 125 MHz.

Table 2-1. 7220A Front Panel Controls, Indicators, and Connectors (cont)

REF. NO.	NAME	FUNCTION	
		.1 FILT	Enables Channel A measurement of signals from 10 Hz to 100 kHz by switching in a 100 kHz Low Pass Filter.
		RES MULT	If the -351 Option is installed, this position enables the 10 kHz resolution multiplier and changes the scale of the RESOLUTION control. The 100 kHz Low Pass Filter is switched in. If the -351 Option is not installed, selection of this mode will prevent the instrument from counting.
10	RESOLUTION Control	Four-position slide switch which allows resolution selection of 100 Hz, 10 Hz, 1 Hz, or .1 Hz. If the -351 Resolution Multiplier Option is installed, the range of resolution is extended to include .01 Hz, .001 Hz, and .0001 Hz selections, and is color-coded by a blue band with the appropriate Function control position. Moving the slide switch between positions automatically generates the instrument's Reset command.	
11	RESET	Pushbutton switch that resets the counters and zeros the display. The number 888888888 is displayed while the button is pressed to allow a visual check of the LED display segments.	
12	POWER switches	These two push-push switches allow selection of instrument power source.	
		BAT/LINE	If the -010 Battery Option is not installed, this switch will not affect instrument operation. If the -010 Battery Option is installed, this switch allows selection of either battery or line power.
		ON/STBY	The ON position enables normal operation. The STBY position powers the oven (with rear panel REF switch set to INT) and battery charging circuits if these options are installed.

2-18. OPERATING NOTES

2-19. The following paragraphs provide information which should be considered before operating the 7220A. This includes information about basic frequency counter operation and descriptions of the 7220A operating modes.

2-20. AC Line Connection

2-21. The input power cord is a three-pin polarized connector which permits connection through the rear panel power receptacle to any of the power voltages described under Input Power. Ensure that the ground pin is connected to a high quality earth ground.

2-22. Maximum Input Levels

CAUTION

To prevent instrument damage, do not connect the active lead of the input signals to the shell of the BNC connector. All BNC connector shells on the 7220A are tied directly to earth ground through the power plug.

2-23. Three of the four BNC connectors on the 7220A are designed to accept signal inputs. Two are on the front panel and allow input signals to be ac-coupled to the two input channels. The third input connector is on the rear panel and is the EXT REF input. Refer to Table 2-4 for the maximum signal input levels.

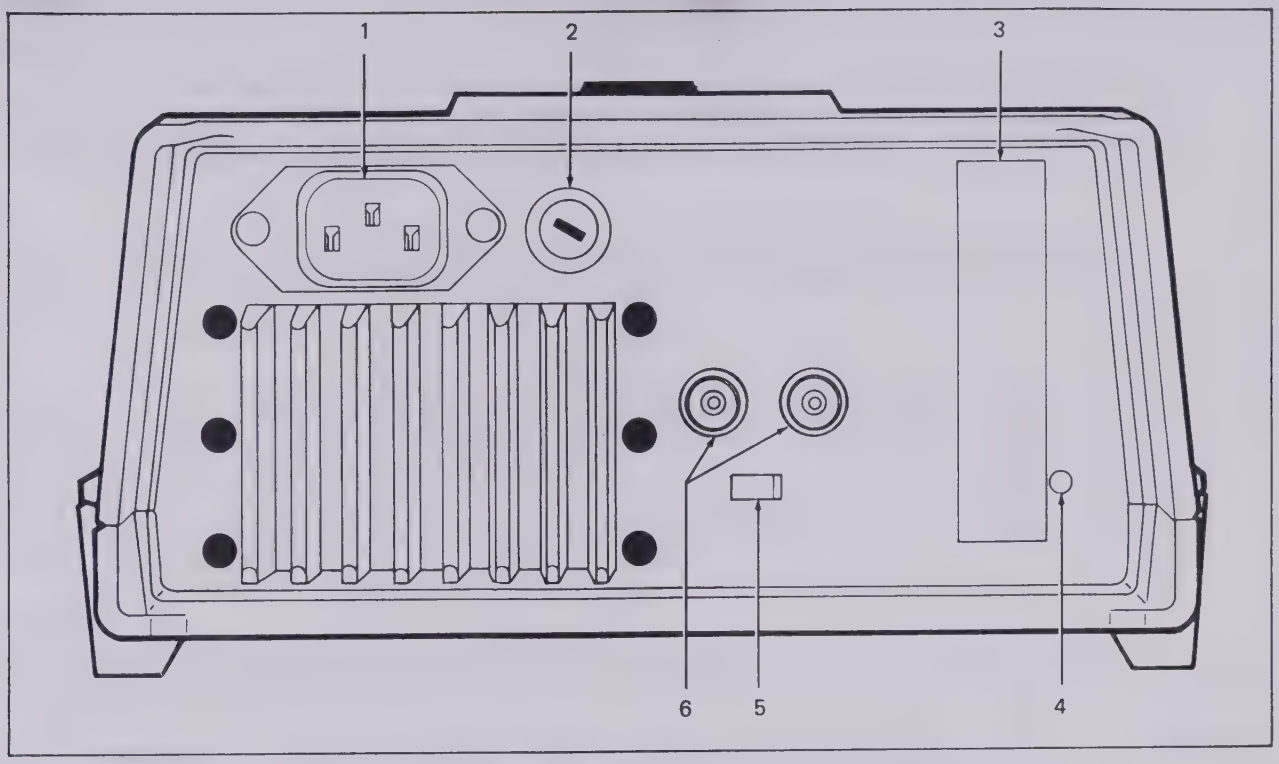


Figure 2-3. 7220A Rear Panel Controls, Indicators and Connectors

Table 2-2. 7220A Rear Panel Controls, Indicators, and Connectors

REF. NO.	NAME	FUNCTION
1	Input Power Connector	A 3 prong receptacle for ac line input.
2	F1	Fuse holder that houses the ac line power fuse and allows easy access for fuse replacement.
3	DATA OUT OPT. -521	Connector location for the Digital Interface, Option -521. When the -521 is not installed, the hole is covered by a removable panel.
4	FREQ ADJ OPT. -111	If the Option -111 time base is installed, this is the access point for adjusting the TCXO frequency. This adjustment is made during calibration only.
5	INT/EXT REF Switch	Two position slide switch that determines whether the instrument is clocked by the 10 MHz internal timebase (INT position), or by an external timebase (EXT position) connected to the 10 MHz REF IN connector rear panel.
6	10 MHz REF	
	IN	BNC connector for connecting an external timebase. This input is used only when the INT/EXT REF switch is in the EXT position.
	OUT	BNC connector which allows access to the timebase signal being used by the instrument.

Table 2-3. Counter Terminology

Attenuation

Attenuation is used to limit the input signal within the dynamic range of the input amplifier. The 7220A has two attenuators for use with Channel A. One allows variable attenuation from X1 to X10, and the other allows step attenuation from X1 to X10. They can be used separately or in combination to provide total attenuation from X1 to X100.

Gate Time

Gate time refers to the length of time during which an input frequency is being counted for display. In the 7220A, the gate time is determined by the resolution selected (see Table 2-5). The greater the degree of resolution, the longer the gate is open.

Hysteresis

In frequency counters such as the 7220A, proper counting requires a pulsed output from the input circuitry. To form this pulse, each input waveform (regardless of its shape) triggers a Schmitt trigger in the input circuit at predetermined triggering or hysteresis levels. An input waveform must pass through both of these hysteresis levels for the input circuitry to generate a pulse. The voltage difference between the two levels is termed the hysteresis window; the minimum signal that can trigger both levels therefore defines the sensitivity of the instrument. Generation of the hysteresis window and sensitivity is illustrated in Figure 2-4.

Input Impedance

The input impedance is the impedance seen by a signal source. Input impedance on Channel A is 1 megohm, shunted by 60 picofarads. Input impedance on Channel B is 50 ohms.

Linear Operating Range

The linear operating range refers to the excursions of the input signal that can reliably trigger the input amplifier without distortion. The linear range of the 7220A varies between the smallest signal level acceptable by the input amplifier (minimum) and the largest attenuated signal that will not be clamped by the input circuits in the amplifier (maximum). The minimum is defined by the sensitivity specifications of the instrument. Operation within maximum levels for Channel A may be ensured through proper use of the ATTENUATION controls.

Prescaling

This is a method of extending the frequency measuring range of a frequency counter by dividing the input signal before it enters the main gate. Thus, a lower-frequency signal is obtained which is coherent with the input signal, and lies within a range which the counter can accept. In the 7220A, the input signals to Channel B are prescaled (or divided) by a factor of 16. To compensate for this, gate times are increased by this same factor so that the counter will still obtain and display an accurate count for the high frequency range.

Resolution

This is defined as the smallest increment of frequency recognized by the counter and thus, the smallest displayed unit in a measurement. In the 7220A, this unit (the least significant digit, or LSD) is defined by each combined setting of the CH A/CH B and RESOLUTION controls.

Sensitivity

This is defined as the minimum specified input signal assured of triggering the instrument, and thus being reliably counted. This specification is related to the hysteresis window, temperature, and the characteristics of the amplifier. See hysteresis.

Trigger Level

This is defined as the voltage level nominally halfway between the upper and lower hysteresis levels. Trigger level is set at 0V in the 7220A and is not adjustable.

Table 2-4. Maximum Input Levels

INPUT TERMINAL	FREQ. RANGE	MAXIMUM INPUT
Channel A (See chart in Specifications, Table 1-3)	10 Hz to 5 KHz 5 KHz to 2 MHz 2 MHz to 125 MHz	250V rms Value linearly decreases from 250V rms at 5 kHz to 5V rms at 2 MHz. 5V rms
Channel B	100 MHz to 1300 MHz	5V rms
EXT REF		3V rms

2-24. Counter Terminology

2-25. Table 2-3 contains definitions which are useful in understanding how and when to use the 7220A controls. These terms are used throughout the manual.

2-26. ACCURACY

2-27. The following paragraphs discuss some of the possible sources of error when making frequency measurements, and some techniques for minimizing these errors.

2-28. One Count Error

2-29. The one count ambiguity, inherent in any gate and counter type of frequency meter, results from an out-of-phase relationship between the pulse train of the input circuit and the pulse train from the timebase. The effect is demonstrated in Figure 2-5. Both Signal A and Signal B have a frequency of 9.5 Hz. But over the same gate time of 1 second, the in-phase Signal A accumulates 10 counts, while the out-of-phase Signal B accumulates only 9 counts. This ambiguity can show up in the measurement as an error of ±1 count. Since this affects the least significant digit (LSD) of the measurement, the one count error can be reduced by selecting a greater degree of resolution. The error caused by this is calculated as follows:

$$\text{Error} = \pm 1/\text{Input Frequency}$$

2-30. Signal Noise, Attenuation, and Filtering

2-31. The extreme sensitivity of the input circuitry of the counter can cause inaccurate counting if there is a significant amount of noise on a large signal. Figure 2-6a shows how this can occur. The input signal is much larger than is needed to transit the hysteresis, and the high frequency noise that is riding on the input signal is of a large enough amplitude that it can also transit the hysteresis window. This causes the extra count shown in Figure 2-6a. This extra count can be eliminated by proper use of the attenuation controls. As illustrated in Figure 2-6b, the input signal and the noise have been attenuated so that the noise does not transit the hysteresis window and correct counting takes place.

2-32. Incorrect counting can also take place if the input signal is overattenuated. In this case, the input signal may be reduced so that it does not always transit the hysteresis window, thus leaving out counts. This is often indicated by an unstable, fluctuating display.

2-33. If the Channel A input signal being measured is below 100 kHz, the 100 kHz low pass filter can be used to eliminate noise that is above 100 kHz. This filter is switched into the Channel A input circuit whenever the front panel CH A/CH B FILT .1 MHz mode is selected, or the Resolution Multiplier Option -351 is installed and the CH A/CH B RES MULT mode is selected.

2-34. Time Base Error

2-35. All crystal oscillator time bases drift in frequency and are thus subject to error. This frequency drift is due to fluctuation in temperature, fluctuation in line voltage, and crystal aging. These effects can be compared in the specification table in Section 1 of this manual. The greatest error is due to temperature fluctuation. This can be reduced by maintaining a stable temperature in the environment in which the instrument is being used. Consideration should be given to the proximity and temperature fluctuation of other instruments, particularly when stacking instruments. The instrument should also be allowed proper warmup time (typically 10 minutes)

2-36. Another way to reduce time base error due to temperature fluctuation is to install one of the optional time bases described in Section 6 of this manual. Option -111 is designed with a temperature compensating element to improve accuracy, and Options -131 and -132 house the crystal in an oven to minimize temperature changes. Time base error can also be reduced by using an

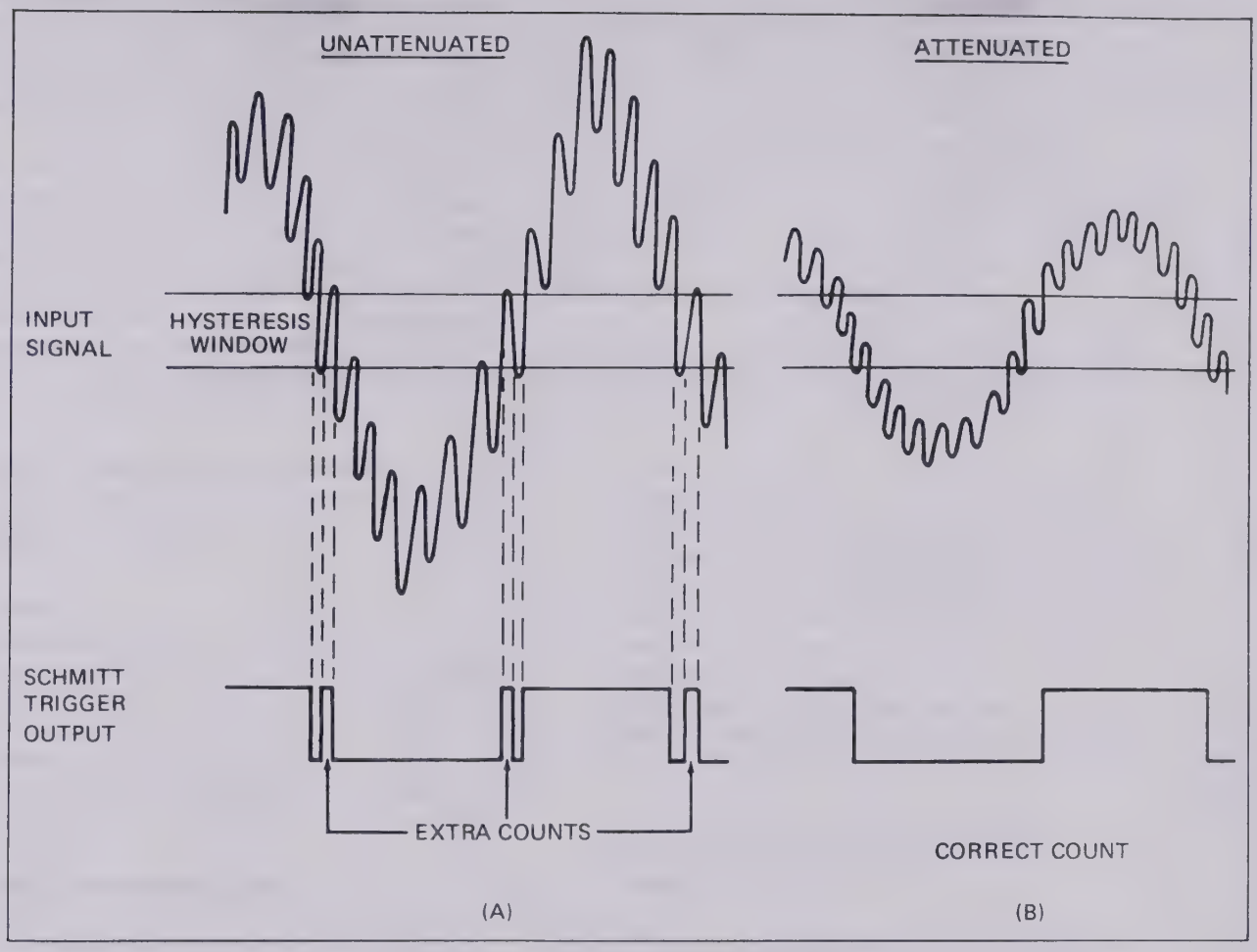


Figure 2-6. Signal Noise and Attenuation

2. Set the CH A/CH B switch to the 125 MHz position.

3. Set the RESOLUTION switch to the desired resolution.

4. Adjust the ATTENUATION controls to obtain a stable display. Attenuating the signal to just above instrument sensitivity will reduce false triggering to a minimum while leaving signal strength high enough to ensure positive triggering.

5. If the input signal is below 100 kHz, eliminate high frequency noise by setting the CH A/CH B switch to the FILT .1 MHz position.

6. If the Option -351 Resolution Multiplier is installed and higher resolution is desired for signals below 10 kHz, move the CH A/CH B switch to the RES MULT position. The RESOLUTION switch is now scaled up by a factor of 1000 so that the 100 Hz, 10 Hz, 1 Hz, and .1 Hz resolution settings are now .1 Hz, .01 Hz, .001 Hz, and .0001 Hz respectively. The Option -351 Resolution settings and the Hz measurement unit are color-coded to the RES MULT position by a blue band on the front panel.

7. Read the frequency on the display and observe the units of measurement (MHz or Hz) to the right of the display. The OVFL annunciator should not be illuminated.

2-45. Frequency Measurements — CHANNEL B

2-46. Frequencies from 100 MHz to 1300 MHz can be counted and directly displayed using Channel B. Use the following procedure:

1. Connect the input signal to the Channel B BNC connector.

2. To measure continuous wave signals, set the CH A/CH B switch to the 1300 MHz position. Measurements are taken consecutively, and the display is updated continuously.

3. To measure burst signals, set the CH A/CH B switch in the BURST position. The first burst signal that arrives at the input triggers one measurement cycle, and this measurement is displayed without being updated. Subsequent measurement cycles are held off while in the burst mode until the signal level on the input is reduced below the Channel B reference threshold level. This prepares the counter to receive, measure and display another burst signal. If the signal carrier level between bursts is greater than the Channel B reference threshold level, it will be necessary to externally attenuate the signal being measured to accomplish this. To measure burst signals, bursts must be present for at least 40 ms + gate time, where gate time = 16 Resolution. For gate times, see Table 2-5.

Table 2-5. Resolution Settings and Gate Times

Resolution Setting (Hz)	100	10	1	0.1
Resolution Multiplier Setting - Channel A only (Hz)	0.1	0.01	0.001	0.0001
Gate Time (sec) — Channel A . . .	0.01	0.1	1	10
— Channel B . . .	0.16	1.6	16	160

2-47. Self Check Mode (CHK)

2-48. The self-check function is used to verify the overall operation of the counter, excluding time base accuracy and the input circuitry. Each setting of the RESOLUTION control provides a predictable display of the 10 MHz reference signal generated by the internal time base. To self-check the 7220A, use the following procedure:

1. Set the CH A/CH B switch to CHK.

2. Momentarily press the RESET control. The display should read 888888888 while RESET is pressed. This resets all the counters and zeros all the display latches.

3. Verify correct display for each of the RESOLUTION settings as defined in Table 2-6.

Table 2-6. CHK Function Display

RESOLUTION SWITCH SETTING	DISPLAY
0.1 Hz	10.0000000 MHz
1 Hz	10.000000 MHz
10 Hz	10.00000 MHz
100 Hz	10.0000 MHz

2-49. Turn Off Procedure

2-50. When the Option -010 Battery Pack is not installed in the 7220A, use the following procedure to turn off the instrument:

1. Set the ON/STBY switch to the STBY position. This will remove power from most of the circuits, but the transformer, regulators, and associated circuitry will still be connected to line power. Also, if either of the two optional oven time bases (Option -131 or -132) is installed, it will receive power if the rear panel REF switch is set to INT. This is indicated by the front panel OVEN annunciator which is illuminated when an oven time base is receiving power. To remove power from an oven time base, set the rear panel REF switch to EXT.

2. To remove line power from the 7220A transformer, regulators, and associated circuitry, disconnect the ac power cord.

2-51. When the Option -010 Battery Pack is not installed, the BAT/LINE switch will have no effect on the operation of the instrument. When the Option -010 is installed, use the turn off procedure outlined above when the BAT/LINE switch is set to LINE. When Option -010 is installed and the BAT/LINE switch is set to BAT, use the following turn off procedure:

1. Disconnect the ac line power cord, if it is not already disconnected.

2. Set the ON/STBY switch to STBY. This will remove battery power from the instrument, but if either of the two optional oven time bases is installed, it will still receive power from the battery if the rear panel REF switch is set to INT. To remove power from an oven time base, set the rear panel REF switch to EXT.

Section 3
Theory of Operation

3-1. INTRODUCTION

3-2. The theory of operation of the 7220A Frequency Counter is presented on two levels. The first is an overall functional description of the 7220A. This is followed by a detailed analysis of the logic and circuits of each major functional element in the counter. The text is supported in this section by functional block diagrams, tables, simplified circuit diagrams, and by the complete instrument schematics in Section 8 of this manual.

3-3. OVERALL FUNCTIONAL DESCRIPTION

3-4. Introduction

3-5. The 7220A Frequency Counter is designed to measure a wide range of frequencies with two possible input channels. Channel A allows the lower range measurement, and includes a selectable 100 kHz low pass filter. Channel B allows higher range prescaled frequency measurement up to 1300 MHz. The Channel B BURST mode allows measurement of high frequency bursts up to 1300 MHz. A self check mode is also provided to check the internal circuitry of the counter. There are several resolution settings that can be selected, as well as an optional resolution multiplier that is fully described in Section 6 of this manual.

3-6. Basic Counter Block Diagram

3-7. To understand the operation of the 7220A, it is helpful to first look at the basic operation of a digital electronic frequency counter. The basic elements of the counter are shown in Figure 3-1. The frequency of a signal can be described by the equation $f = n/t$, where f is the average frequency found by accumulating n cycles of the signal over the time period t. The frequency measurement is accomplished by counting the number of cycles n of the unknown signal over a period t, which is precisely established by a very accurate reference time base and time base dividers. This procedure is illustrated in Figure 3-1.

3-8. The input signal is applied to the signal conditioner which conditions the signal to a form that is compatible with the internal circuitry of the counter. The signal conditioner also shapes the signal into a square wave, which is then presented to the main gate for counting.

3-9. The main gate is the heart of the counter, for when it is open, it allows the preconditioned input signal to pass through and be counted. In some counters, there is a separate logic gate whose only function is to serve as the main gate. In the 7220A, however, the main gate function is served by the First Counter flip flop in the counter series. To "open" or "close" the main gate actually means this First Counter FF is being enabled or disabled. The amount of time the First Counter FF is enabled is called the gate time. The First Counter FF is enabled or disabled by the main gate flip flop which responds to output pulses from the time base dividers.

3-10. The events required to make a frequency measurement occur as follows: The operator selects the measurement resolution desired. This tells the time base dividers how long the First Counter FF is to be enabled, or in other words, what division factor to apply to the time base reference frequency. The time base dividers trigger the main gate flip flop which enables the First Counter FF, beginning the gate time. While the counters count the unknown frequency, the time base dividers divide the reference frequency by the factor selected. When this is completed, the main gate flip flop is triggered again. This disables the First Counter FF, ending the gate time, and the measured signal is displayed. The timing for these events is presented in Figure 3-1.

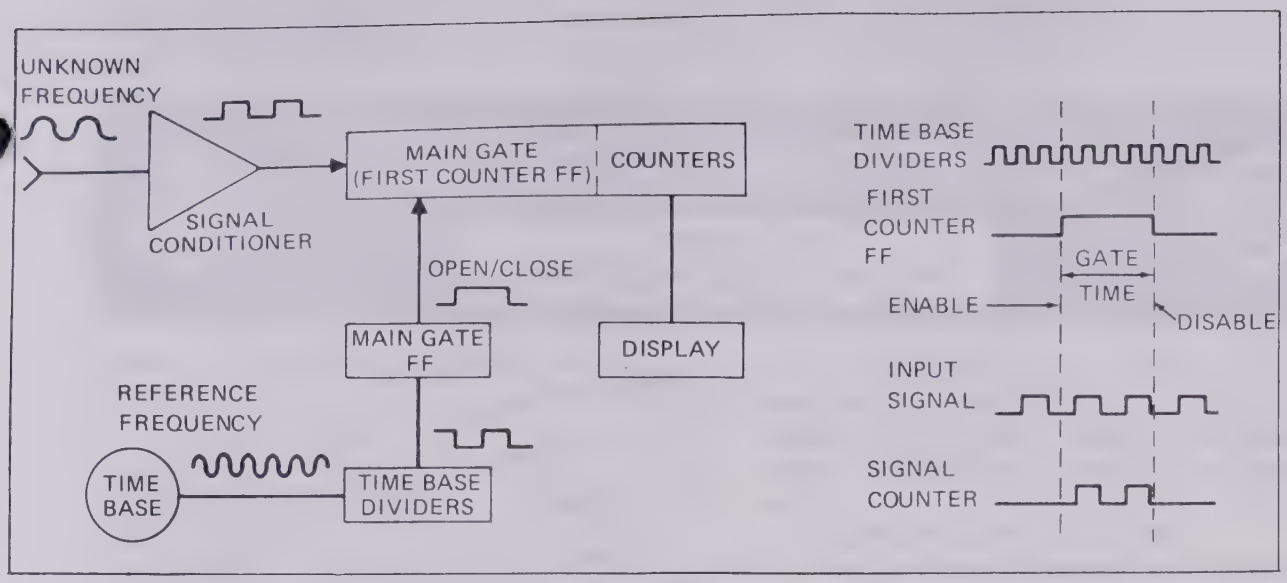


Figure 3-1. Basic Counter Block Diagram

3-11. FUNCTIONAL BLOCK DIAGRAM

3-12. Major functional areas of the 7220A are shown in Figure 3-2. The operation of each block is described in the following paragraphs.

3-13. Measurement Controls

3-14. The measurement controls consist of the Resolution Control and the Function Control. These are the front panel RESOLUTION and CH A/CH B slide switches, and their function depends on the position of the switch. The Resolution Control supplies decimal point placement information to the display decoder, and measurement range information to the main time base divider. The Function Control supplies mode selection information to the Control Logic and the Input Select.

3-15. Control Logic

3-16. The Control Logic governs the sequence of events in the counter, including the time base division and counting. It receives information from the Function control, including burst and reset modes. It generates reset commands for the Main Time Base Divider and the accumulators, and it clears the Main Gate Flip Flop. It also generates the strobe command for the display latches.

3-17. Time Base and Dividers

3-18. The Time Base generates the 10 MHz reference signal which is used to provide the precise timing needed for the internal signal counters. The 10 MHz is generated by the standard internal oscillator, one of the optional TCXO or oven oscillators, or by an external time base whose signal is applied at the rear panel of the instrument. The Time Base Dividers receive measurement range instruction from the Resolution Control. They divide the 10 MHz by the proper amount to provide the Control Logic and First Counter FF with the proper timing needed to generate the actual required gate signal.

3-19. First Counter Flip Flop and Main Gate Flip Flop

3-20. As mentioned in the previous section on the basic counter block diagram, some counters have a separate logic gate (sometimes called the "main gate") whose only function is to allow or prevent passage of the unknown frequency into the counters to be counted. In the 7220A, however, this main gate function is served by the First Counter FF, which is the first counter in the counter series. While the First Counter FF is enabled, the unknown frequency is counted, but while it is disabled, no counting takes place. The interval during which the First Counter FF is enabled is called the gate time. The First Counter FF is enabled or disabled by the Main Gate FF, which operates through the Gate Synchronizer FF. The First Counter FF responds to instructions from the Control Logic and the Time Base Dividers.

3-21. Counters

3-22. There are nine decade BCD counters that tally the number of counts received while the First Counter FF is enabled, and present the information to the Display Latch and Multiplexer function. The first decade BCD counter is actually a series of four flip flops, the first of which is the First Counter FF described above.

static awareness

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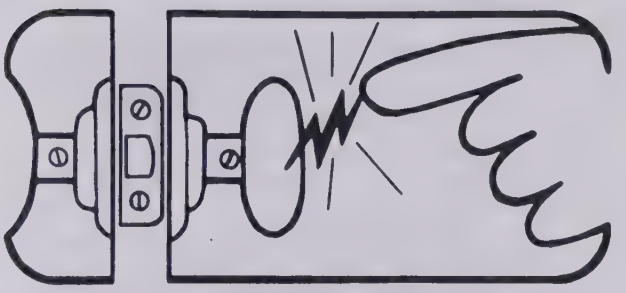

Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
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3. Using the procedures, and packaging and bench techniques that are recommended.

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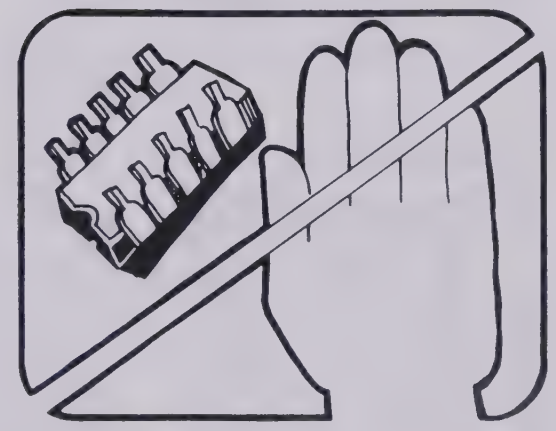
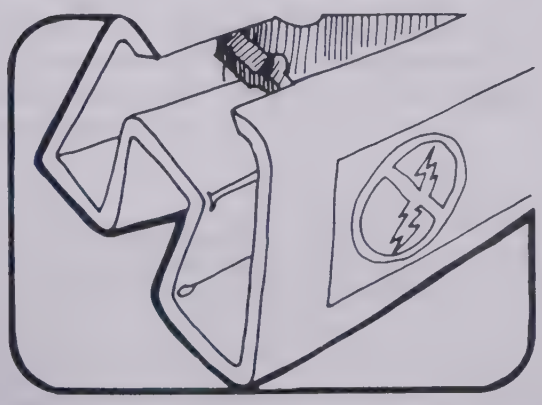
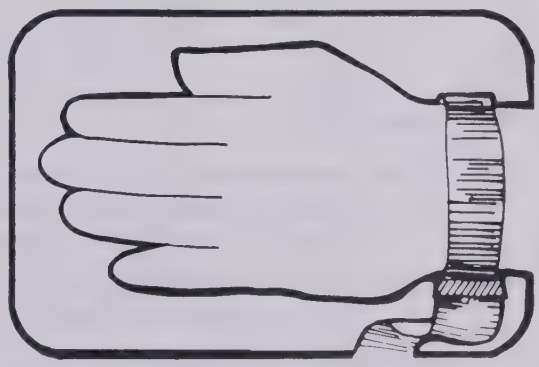


1. MINIMIZE HANDLING



2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



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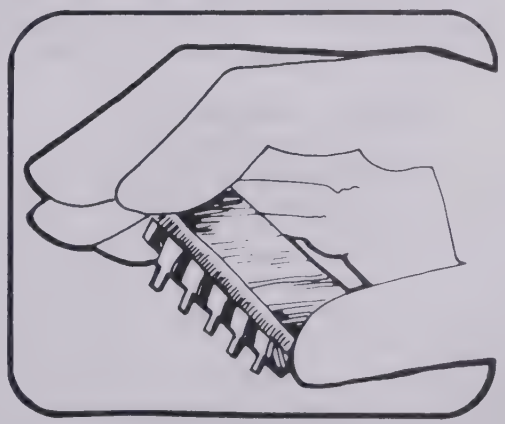
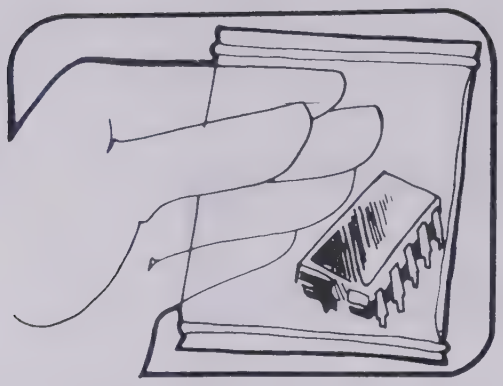
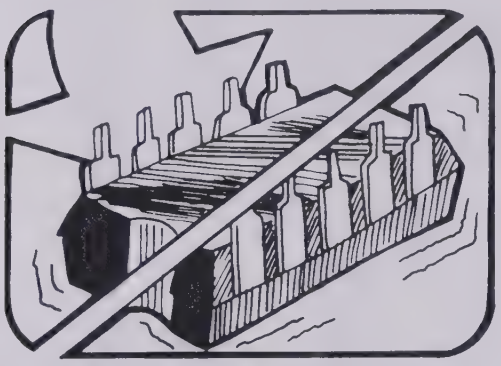


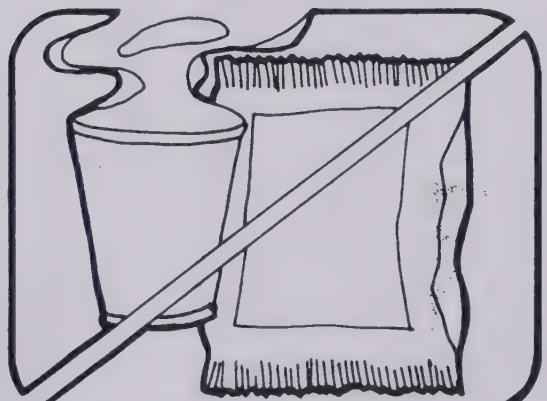
4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



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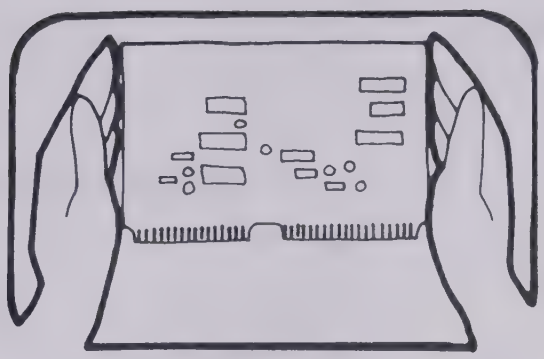
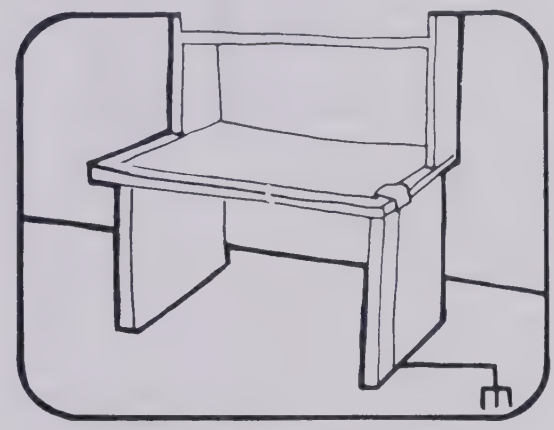


8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
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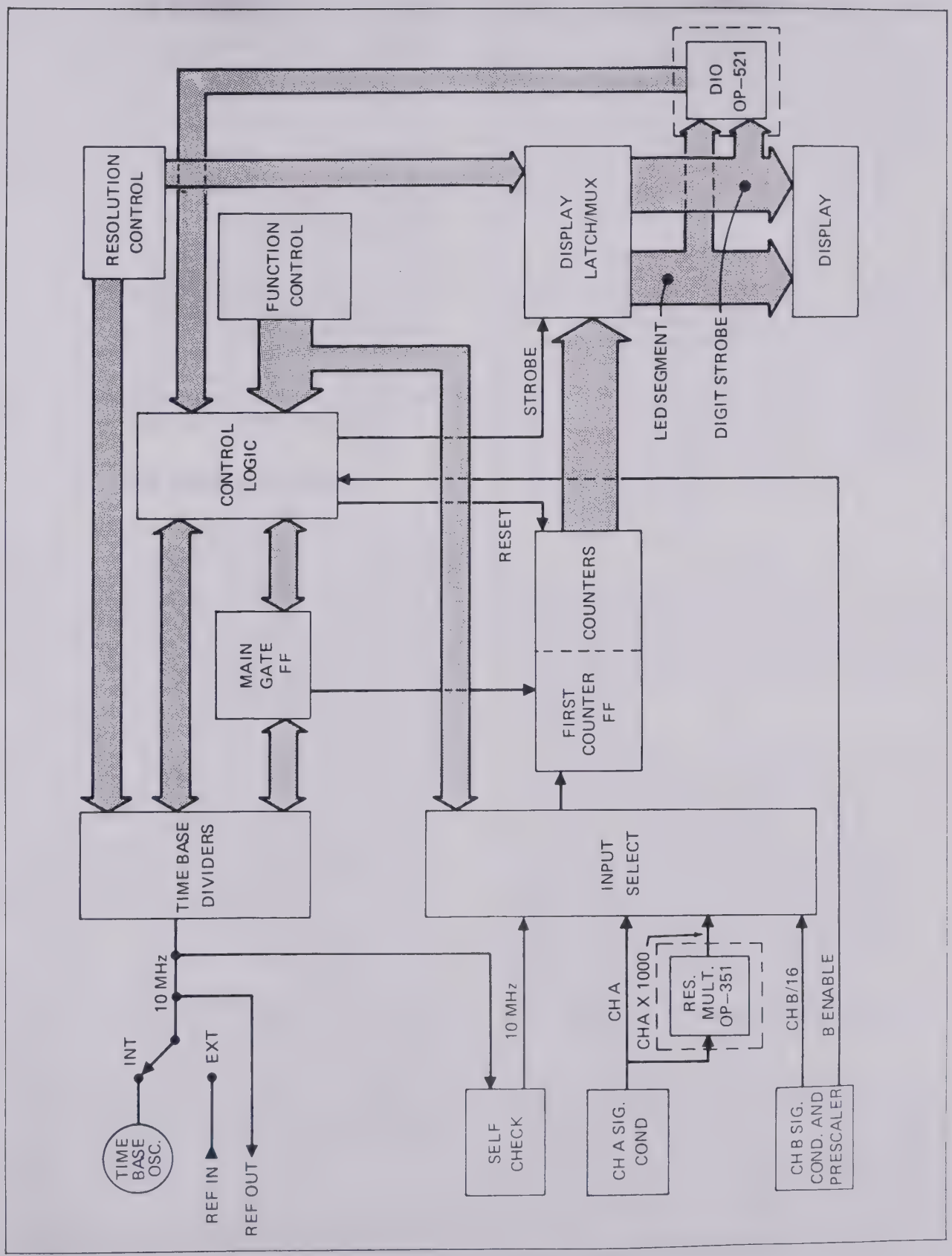


Figure 3-2. 7220A Functional Block Diagram

3-43. Since the 7220A has no separate ac power switch, ac power is always applied to the transformer, bridges, and regulators when the power cord is connected. When the ON/STBY switch is in the ON (depressed) position, power is supplied to the internal circuits. When the ON/STBY switch is in the STBY position, power is removed from the internal circuits, but is supplied to any optional oven time base that is installed (when the rear panel REF switch is set to INT) to eliminate the need for oven warm-up time. The front panel OVEN LED annunciator indicates that an oven time base is receiving power.

3-44. The regulated +5V line passes to the front panel BAT/LINE switch. When the Battery Pack Option -010 is not installed, the position of the BAT/LINE switch has no effect on instrument operation. Refer to Option -010 in Section 6 for a discussion of the battery option circuitry. The Channel B high speed counter -1.8V voltage regulation is described in the Channel B Signal Conditioner section.

3-45. Channel A Signal Conditioners

3-46. The Channel A signal conditioners consist of voltage divider attenuators, current limiters, a high impedance FET buffer, and a preamplifier IC that consists of a differential input amplifier, a Schmitt trigger, and ELC and TTL logic drivers. As can be seen in Figure 3-3, the Channel A signal enters at the front panel BNC and passes to the main voltage dividers, resistors R1 and R2, which provide attenuation of X10. The X10 attenuation can be selected by positioning the front panel ATTENUATION slide switch. The signal then passes through the current limiting and clamping network consisting of resistors R3 and R4, and diodes CR1 and CR2. This limits the signal presented to the gate of the high impedance buffer, FET Q1, to 1.2V p-p. Q1 is a low frequency device, so capacitor C5 provides a high frequency path around it. The signal is ac-coupled through C6 to one input of the differential input amplifier on the preamp IC, U1. A dc return path is provided by R7.

3-47. PREAMP IC

3-48. Most of the signal conditioning takes place in the preamp IC U1. U1 is enabled by the front panel Function control when one of the three Channel A modes is selected, and is off when Channel A is not in use. U1 requires +5V and -5V power supplies for operation. The +5V supply passes through choke L1 before arriving at U1. The -5V supply is obtained from the three terminal regulator U2, which drops a -12V supply to the required -5V

3-49. The amplifier in U1 has a dynamic operating range which is well beyond the 1.2V p-p range allowed by the signal clamps R3, R4, CR1 and CR2. Normally, the amplifier has a 3 dB bandwidth which ensures adequate handling of Channel A's 10 Hz to 125 MHz input signal range. For low frequency signals, however, a low pass 0 to 100 kHz filter can be switched in by selecting front panel CH A/CH B position CH A FILT (if the Resolution Multiplier Option -351 is installed, the CH A RES MULT position will also switch in the filter). This turns on transistor Q2, which switches capacitor C12 into the amplifier circuit. The value of C12 determines the low pass filter bandwidth, which in this case is 100 kHz.

3-50. The amplifier trigger level is adjusted by potentiometer R10. The R10 setting is an internal adjustment, and is adjusted during instrument calibration to compensate for the amplifier offset. This procedure can be found in the Calibration Adjustments in Section 4. Variable attenuation of Channel A signals can be achieved by adjusting R12, which controls the gain of the amplifier. R12 is actually the upper attenuation control which is accessible from the 7220A front panel. R12 allows a variable attenuation range up to X10, and when used in conjunction with the X10 step attenuator, allows a total attenuation range of X100.

3-51. SCHMITT TRIGGER

3-52. As can be seen in Figure 3-3, the signals pass from the amplifier to the Schmitt trigger, where the waveform is shaped into a pulse train suitable for counting. The width of the hysteresis window can be varied by adjusting R11. This is an internal adjustment, and proper adjustment procedure is described in the Calibration Adjustments in Section 4.

3-53. The ECL driver on U1 drives Channel A ECL (thus the mnemonic AECL) and complementary ECL ($\overline{\text{AECL}}$) logic level signals to the Input Select for counting. The TTL driver is powered only when the CH A/CH B switch is in the RES MULT mode, and it provides Channel A TTL (ATTL) logic level signals for the Resolution Multiplier Option -351. The Resolution Multiplier multiplies the low frequency signals by 1000, and presents the X1000 signal to Input Select for counting, thus increasing signal resolution. Resolution Multiplier operation is described more fully in Section 6.

3-54. Channel B Signal Conditioners and Prescaler

3-55. The 100 MHz to 1300 MHz Channel B signals are amplified, prescaled (divided by 16), and buffered before being presented to the 7220A Main Gate for counting. As can be seen in Figure 3-4, the amplification and first stage of frequency division takes place in the hybrid, U4. Also shown in Figure 3-4 is the threshold detect circuitry which indicates whether a valid Channel B input signal is present or not, and a tracking regulator which maintains a constant 6.8V across the signal dividers.

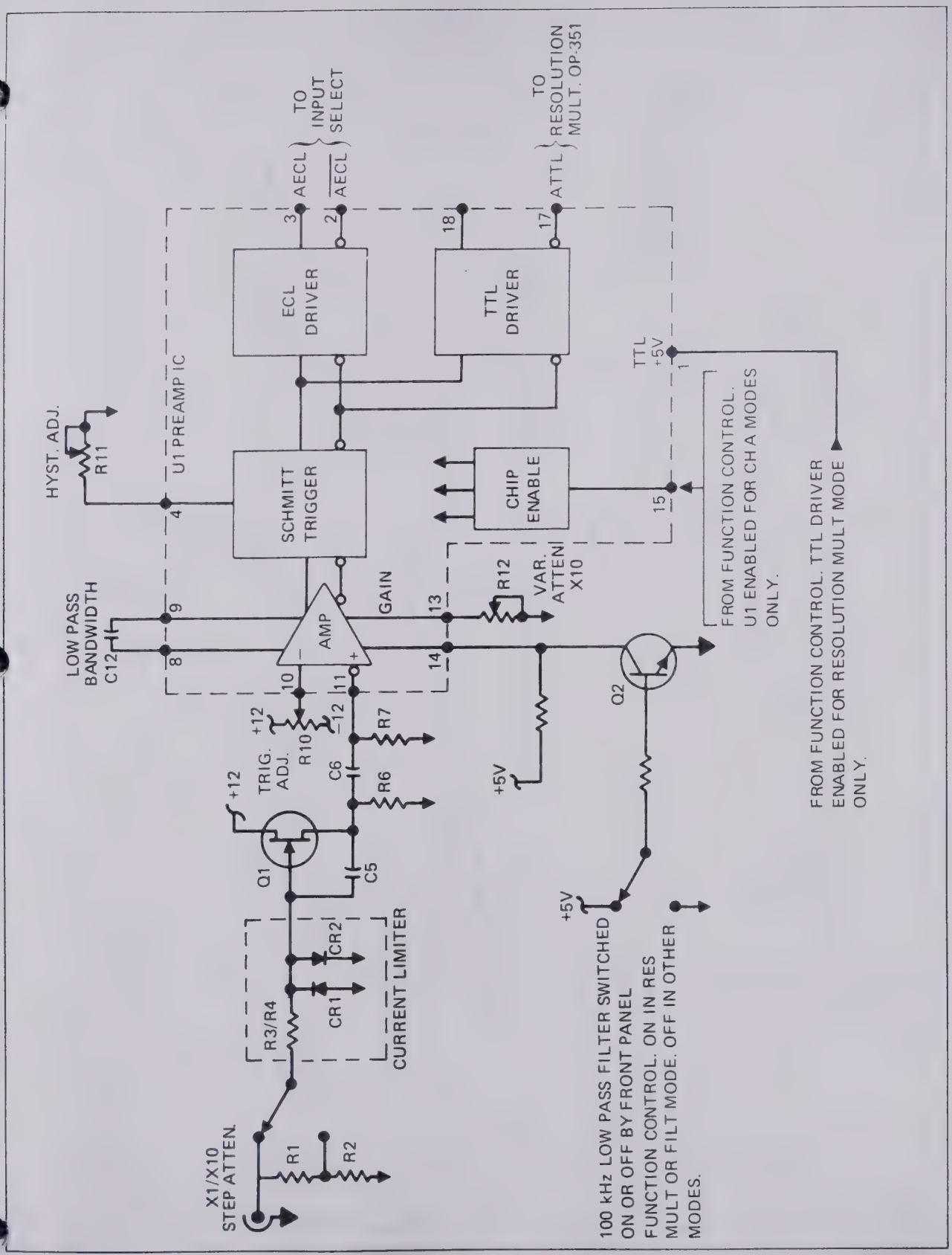


Figure 3-3. Channel A Signal Conditioners

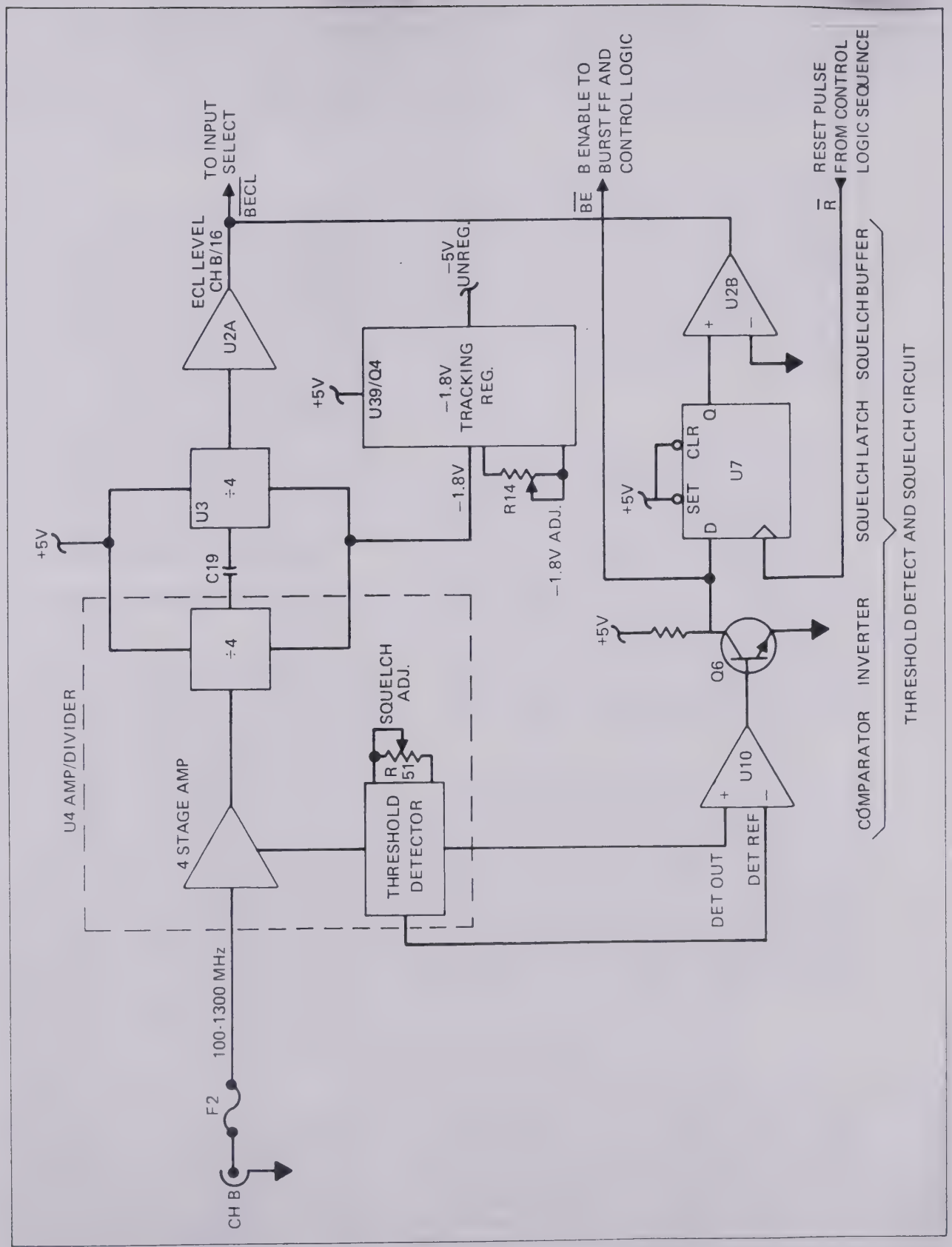


Figure 3-4. Channel B Conditioners and Prescaler

3-56. The Channel B input signals enter through the front panel BNC connector and pass through fuse F2, which provides voltage overload protection for the input circuitry. A spare, unconnected fuse, F3, is also located on the main PCB. The signals enter the high frequency four-stage amplifier on U4. The amplifier provides approximately 40 dB gain, and presents the signal to the high speed divider on U4 for prescaling.

3-57. PRESCALING

3-58. The purpose of prescaling is to extend the measurement range of the frequency counter by prescaling or dividing the input signal down to the operating range of the counters in the frequency counter. To compensate for this signal division, the First Counter FF is enabled longer so the proper number of counts are accumulated. This is described in detail in the theory of operation regarding the time base dividers. The Channel B 100 MHz to 1300 MHz input signals are prescaled by a factor of 16. This is accomplished by a very high speed divide-by-four ECL prescaler mounted on the hybrid, U4, and a second divide-by-four ECL prescaler, U3. The two prescalers are ac-coupled, and are shown in Figure 3-4. U3 has complementary outputs that provide ECL level signals to U2A, which buffers them, and presents the Channel B ECL level ($\overline{\text{BECL}}$) signal to the Input Select.

3-59. HIGH SPEED COUNTER VOLTAGE REGULATION

3-60. The high speed divide-by-four prescalers (one is mounted on the hybrid U4, and the other is U3) are sensitive to voltage fluctuation, and must be supplied with a constant 6.8V to operate properly. This is particularly important if the 7220A is being operated with batteries, since the voltage supply levels will sometimes drop. The 6.8V voltage regulation is accomplished by the tracking regulator U39 and transistor Q4. U39 tracks the +5V supply line, and operates with Q4 to supply the two prescalers with a constant 6.8V below the +5V line (or -1.8V). The 6.8V difference can be calibrated by adjusting potentiometer R14. See the Calibration Adjustments section in Section 4 for the proper procedure. When the 7220A front panel CH A/CH B switch is not in either of the two Channel B modes, transistor Q5 acts as a power switch that turns off U39, and transistors Q2 and Q3 act as power switches to remove the +12 supply from U4. Thus the Channel B input circuitry is off when not in use.

3-61. THRESHOLD DETECT CIRCUIT

3-62. In the absence of an input signal, the high-speed divide-by-four prescaler on U4 will oscillate, thus supplying an erroneous signal which would be counted and displayed by the frequency counter if not eliminated. To prevent this from happening, a threshold detect circuit is provided which determines whether an input signal is being applied that is above a preset reference level or threshold. If an input signal is above the threshold, then it is allowed to pass on through to the Input Select for counting and display. If, however, the input signal is below the threshold, the oscillation signal is squelched, or suppressed, and not allowed to pass through to the Input Select.

3-63. As can be seen in Figure 3-4, the threshold detect circuit begins on the hybrid, U4. U4 contains the threshold detector circuitry which tops the input signal between the third and fourth amplifier stages and passes a detector out level (Det Out) and a detector reference level (Det Ref) to the inputs of the comparator U10. The threshold or detector reference level is determined by the setting of a potentiometer, the Squelch Adjust, which is located on U4. The correct procedure for setting the Squelch Adjust can be found in Section 4 under Calibration Adjustments.

3-64. U10 compares Det Out with Det Ref. Either of two situations can arise: In the first case, if the Det Out is more positive than the Det Ref (indicating a signal above threshold), the output of U10 is high. Transistor Q6 inverts the high by turning on, thus presenting a logic low to the D input of U7, an edge-triggered D flip flop. Since both set and clear are tied high, U7 presents a logic low to the buffer U2B when it is clocked by a Reset pulse from the Control Logic Sequencer. U2B produces an ECL low signal which is tied to the output of buffer U2A. Since the outputs of U2A and U2B are wired together, they form a logic OR. In this case, with an ECL low signal from U2B, the prescaled Channel B signal ($\overline{\text{BECL}}$) from U2B passes through unhindered to the Input Select circuitry.

3-65. In the second case, however, the outcome is just the opposite. When the Det Out is less positive than the Det Ref, (indicating a signal is below threshold), the output of the comparator is low. Q6 inverts this to a high, which is passed by the D flip flop to buffer U2B. U2B produces an ECL high signal which is joined to the U2A output. This ECL high overrides any erroneous signal from the freely oscillating prescaler. Thus, until a valid input signal is present, no signal will be counted or displayed. The function of the B Enable ($\overline{\text{BE}}$) is described in the section on the Control Logic Sequencer.

3-66. Input Select

3-67. There are four possible input sources to the 7220A First Counter FF. As can be seen in Figure 3-5, each of the four possible sources are applied to one of the NOR gates on U8, a quad 2-input NOR gate. The gate sources are the prescaled Channel B signal (CH B/16), the 10 MHz timebase signal, the Channel A signal with the Resolution Multiplier Option -351, and the Channel A

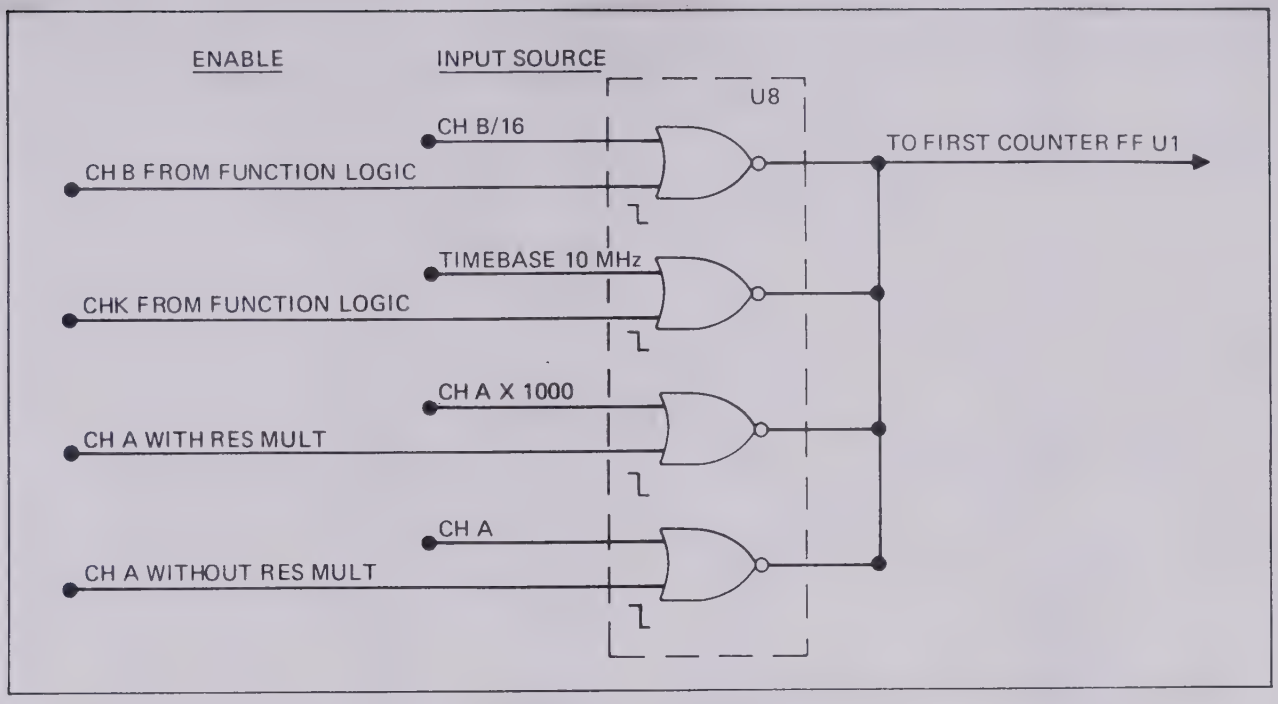


Figure 3-5. Input Sources

signal without the Resolution Multiplier. Depending on which Function is selected by the 7220A front panel CH A/CH B switch, the appropriate source is enabled by a logic low signal from the Function logic, and is applied to the First Counter FF for counting.

3-68. Time Base Dividers

3-69. The 7220A Time Base Dividers provide the accurate timing needed for the gate time intervals, as well as the clock for the Gate Synchronizer, and the scan rate for the Control Logic Sequencer. This is accomplished by dividing the 10 MHz reference signal from the time base according to instructions received from the CH A/CH B and RESOLUTION Controls.

3-70. As shown in Figure 3-6, there are three time base dividers: the Decade Divider, the Binary Divider, and the programmable Main Divider. The Decade Divider receives the 10 MHz time base signal and divides it to 1 MHz and 100 kHz. The 100 kHz signal is sent to the Gate Synchronizer, and is explained in the section about the Gate Synchronizer. The 1 MHz can follow one of two paths, depending on which Function is selected on the 7220A front panel Function Control switch. For Channel A modes, the 1 MHz is sent directly to the Main Divider.

3-71. For Channel B modes, the 1 MHz goes first to the Binary Divider where it is divided by 16 before being sent to the Main Divider. The 1/16 MHz division compensates for Channel B signal prescaling. The high frequency input signals coming into Channel B are prescaled (divided) by a factor of 16 to the operating range of the counters. To compensate for this slower input signal, the gate times are increased by the same factor of 16 (see Table 3-1) by dividing the Main Divider clock signal to 1/16 MHz. Therefore, even though the Channel B signal is divided by 16 by the time it reaches the First Counter FF, the gate times are 16 times longer, so the 7220A will count and display the proper frequency. The Binary Divider also provides the 61 Hz Scan Rate for the Control Logic Sequencer, U32, a decade ring counter. The 61 Hz is approximate, for it is actually 1 MHz divided by 2^{14}.

3-72. MAIN DIVIDER

3-73. The actual counting of the gate time intervals takes place in the Main Divider, U20. The Main Divider consists of a series of decade counters which can be selected according to binary code information received on the RNG 1 and RNG 2 lines. RNG 1 and RNG 2 are controlled by the front panel RESOLUTION Control setting, and they select the counting range for U20, and thus the gate time. This operation is outlined in Table 3-1. For example, assume the Resolution selected is 10 Hz. Then RNG 1 will be 1, RNG 2 will be 0, and the U20 will be programmed to count to 100,000. For Channel A mode, the 1 MHz clock is used, so it will take 100,000/1 MHz or 0.1 seconds for U20 to count to 100,000. This 0.1 second time interval is the gate time.

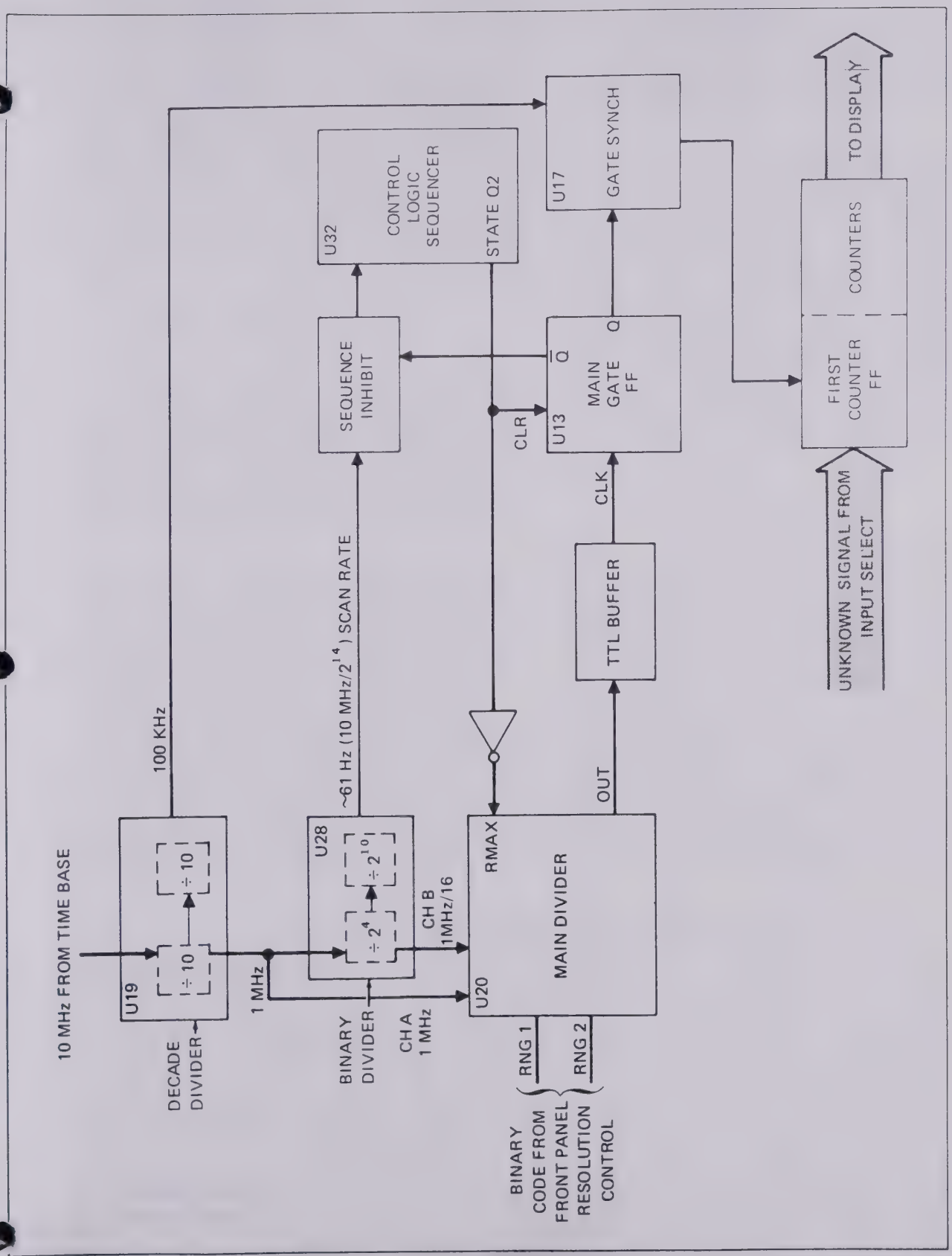


Figure 3-6. Time Base Dividers and First Counter FF

3-74. For Channel B mode, the 1/16 MHz clock is used, so it takes 16 times longer for U20 to count up to 100,000. This means the 10 Hz Resolution gate time is 16 times longer for Channel B than for Channel A, or 1.6 seconds instead of 0.1 second. As can be seen in Table 3-1, the Resolution Multiplier Option -351 does not affect the range or gate times, but instead multiplies very low frequency Channel A signals by 1000, which has the effect of increasing the Resolution by 1000. This is described in detail in the Option -351 information in Section 6 of this manual.

3-75. FIRST COUNTER FF

3-76. The First Counter FF is enabled or disabled by a sequence of events which begins with the Control Logic Sequencer, and involves the Main Divider, the Main Gate FF, and the Gate Synchronizer. The operation of the Control Logic Sequencer is described in detail elsewhere in this section. The timing of the event sequence can be seen in Figure 3-7.

3-77. The event sequence which opens the Main Gate begins with the Q2 pulse from the Control Logic Sequencer. As can be seen in Figure 3-6, Q2 clears the Main Gate FF, and is inverted and applied to the R Max of the Main Divider, U20. When R Max receives a positive pulse, it resets the U20 counters to all 9's. R Max is normally held high, holding the U20 counters at all 9's, but when the inverted (low) Q2 pulse arrives, it releases R Max, allowing the counters to be advanced by the time base clock. On the negative edge of the next clock pulse into U20, the counters advance to all 0's, generating an Out pulse through the TTL buffer (which is needed to raise the U20 MOS signal to TTL) and then on to the Main Gate FF, U13, where it sets the U13 Q output at 1. This is applied to the Gate Synchronizer, which enables the First Counter FF (beginnging the gate time) and allows the unknown signal to pass on to the counters.

3-78. At the same time, the U13 $\overline{Q}$ output goes to 0 and is applied to the Sequence Inhibit (U31, pin 8). The Sequence Inhibit prevents the Sequencer from advancing for the duration of the gate time by holding off the Scan Rate clock. Meanwhile, U20 counts up to the range selected, and when the U20 counters reach their full count and again advance to all 0's, another Out pulse is generated and applied to the Main Gate FF, U13. U13 is a toggle mode, so the Q output toggles to 0. This is applied to the Gate Synchronizer, which disables the First Counter FF (thus ending the gate time) and stops the counting of the unknown input signal. The U13 $\overline{Q}$ output toggles to 1, releasing the Sequence Inhibit, and allowing the Control Logic Sequencer to resume its sequence advance on the next Scan Rate pulse.

3-79. GATE SYNCHRONIZER

3-80. The purpose of the Gate Synchronizer is to restore the time base accuracy to the timing sequence before it reaches the First Counter FF. Since the Main Time Base Divider, U20, is a MOS device, by the time it completes its input clock division and clocks the Main Gate FF, the signal may not be as accurate as the reference time base. The Main Gate FF presents a signal on the D input of the Gate Synchronizer, a D FF, but the Gate Synchronizer does not pass the signal on to the First Counter FF until it is clocked by a 100 kHz signal that comes from the Decade Time Base Divider. This 100 kHz signal has been divided from the 10 MHz reference time base, so time base accuracy is restored to the timing sequence, and the gate times are as precise as the time base signal. This sequence can be seen in Figure 3-7.

Table 3-1. Resolution Control Range and Gate Time

RESOLUTION Setting (Hz) Channels A and B		100	10	1	0.1
RES. MULTIPLIER Setting (Hz) Channel A only		0.1	0.01	0.001	0.0001
RANGE CONTROL	**RNG 1**	0	1	0	1
	RNG 2	0	0	1	1
U20 Main Time Base Division Factor		10^4	10^5	10^6	10^7
GATE TIME (sec.)	**CH A**	0.01	0.1	1	10
	CH B	0.16	1.6	16	160

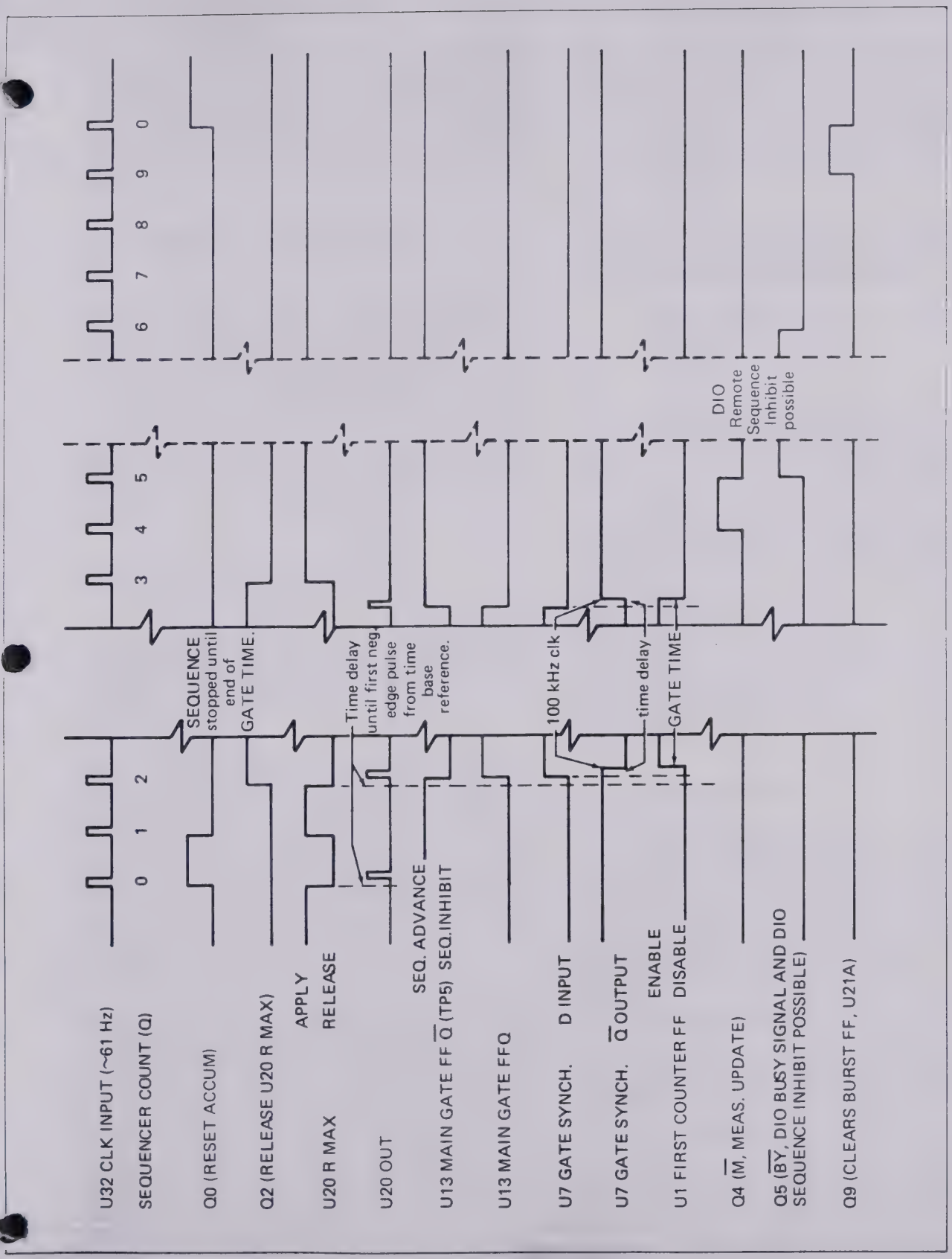

U32 CLK INPUT (~61 Hz)
SEQUENCER COUNT (Q)
0 1 2 3 4 5 6 7 8 9 0
Q0 (RESET ACCUM)
SEQUENCE stopped until end of GATE TIME.
Q2 (RELEASE U20 R MAX)
APPLY
U20 R MAX
RELEASE
Time delay until first neg. edge pulse from time base reference.
U20 OUT
SEQ. ADVANCE
U13 MAIN GATE FF Q̄ (TP5) SEQ.INHIBIT
U13 MAIN GATE FFQ
100 kHz clk
U7 GATE SYNCH. D INPUT
U7 GATE SYNCH. Q̄ OUTPUT
time delay
ENABLE
U1 FIRST COUNTER FF DISABLE
GATE TIME
DIO Remote Sequence Inhibit possible
Q4 (M̄, MEAS. UPDATE)
Q5 (BY̅, DIO BUSY SIGNAL AND DIO SEQUENCE INHIBIT POSSIBLE)
Q9 (CLEARS BURST FF, U21A)

Figure 3-7. Control Logic Timing

3-81. A time delay is present between the time the D input is received and the next edge of the 100 kHz signal clocks the Gate Synchronizer. This same delay occurs at the trailing edge of the gate time. The effect is to bring the gate signal into time sync with the time base clock, and thus remove the time jitter introduced by the MOS divider chain.

3-82. Control Logic Sequencer

3-83. The Control Logic for 7220A operation is provided by the Control Logic Sequencer, U32, a decade ring counter. U32 operation is outlined in Figure 3-8 and Table 3-2, and a timing diagram is provided in Figure 3-7. The Sequencer advances through a ten-step sequence at a Scan Rate of approximately 61 Hz which is provided by the Binary Time Base Divider. Each of the 10 counts (Q0-Q9) has a separate output, and is normally low except during its respective decimal time slot, when it goes high.

3-84. B ENABLE AND BURST FF

3-85. In order to understand the operation of the Control Logic Sequencer, it is necessary to understand the operation of the BURST Logic, which includes the B Enable and the BURST FF.

3-86. When the Channel B BURST mode is selected by the front panel CH A/CH B switch, the 7220A is designed to wait until a signal input above threshold is present on Channel B, then allow one pass through the measurement cycle from Q0-Q9. During this one cycle, it will count and display the input signal, and then hold that display without update until another burst occurs. This is done by enabling the Clock Enable on the Sequencer (CE, U32, pin 13) for one measurement cycle, and then disabling the Clock Enable.

3-87. Disabling the Clock Enable involves the B Enable ($\overline{BE}$) line, which is tied to the collector of Q6 (see Figure 3-4). When a Channel B input signal above threshold is present, comparator U10 is high, turning on Q6, which puts a low signal on $\overline{BE}$. $\overline{BE}$ is then inverted to BE, and BE is applied to the BURST FF, U21A (see Figure 3-8). The high BE clocks U21A, and the U21A $\overline{Q}$ is low, which enables the Clock Enable and allows the measurement cycle to start, beginning at state Q0. At the end of the measurement cycle, the leading edge of the Q9 pulse clears U21A, which sends the U21A $\overline{Q}$ high, disabling the Clock Enable. No further measurement cycles will take place until BE goes low at the end of the burst and then high again with the next burst.

3-88. As can be seen in Figure 3-8, the Function Control supplies the $\overline{BST}$ line to the Set input of U21A. In the BURST mode, $\overline{BST}$ is low and U21A is not set. But in a non-BURST mode, U21A is set by the high $\overline{BST}$, which causes the low $\overline{Q}$ to enable the Clock Enable all the time, thus allowing continuous measurement cycles to occur in non-BURST modes.

3-89. In order for there to be a measurement in the BURST mode, the BURST signal must be present for a minimum length of time (for gate times see Table 3-1):

Minimum Burst = Gate time + 40 ms

3-90. SEQUENCE INHIBIT

3-91. There are two ways of preventing the U32 Sequencer from advancing. One is by means of the Clock Enable input on U32 and the BURST FF as described earlier. The other is by externally disabling the clock. As can be seen in Figure 3-8, the 61 Hz Scan Rate clock is applied to the Sequence Inhibit function. The Sequence Inhibit also has inputs from the Main Gate FF and the Digital Interface Option -521 (DIO). The Main Gate FF disables the Scan Rate clock in state Q2 during the gate time interval. The DIO can disable the Scan Rate clock in state Q5. The Sequencer will then be held in state Q5 until a Reset is generated. The operation of the Main Gate FF is described in more detail in the previous First Counter FF description. The DIO is described in the section on the Sequence Count Cycle (state Q5) and in Section 6 of this manual.

3-92. SEQUENCE RESET

3-93. The high signal on the U32 Reset input will reset the Sequencer to its first (Q0) count. The Reset may be generated by the front panel Reset control, by remote operation through the Digital Interface Option -521, or by an out-of-lock signal from the Resolution Multiplier Option -351. The operation of the options is described in more detail in Section 6 of this manual.

3-94. SEQUENCE COUNT CYCLE

3-95. The count cycle (states Q0-Q9) for the U32 Sequencer is described in the following paragraphs.

3-96. States Q0 and Q1

3-97. The Sequencer U32 count cycle is outlined in Table 3-2. The count cycle begins with the Q0 state. As shown in Figure 3-8, Q0 does several things: it resets the accumulators, it clears U21B, and it applies a low to the R Max on the Main Time Base Divider, U20, releasing R Max.

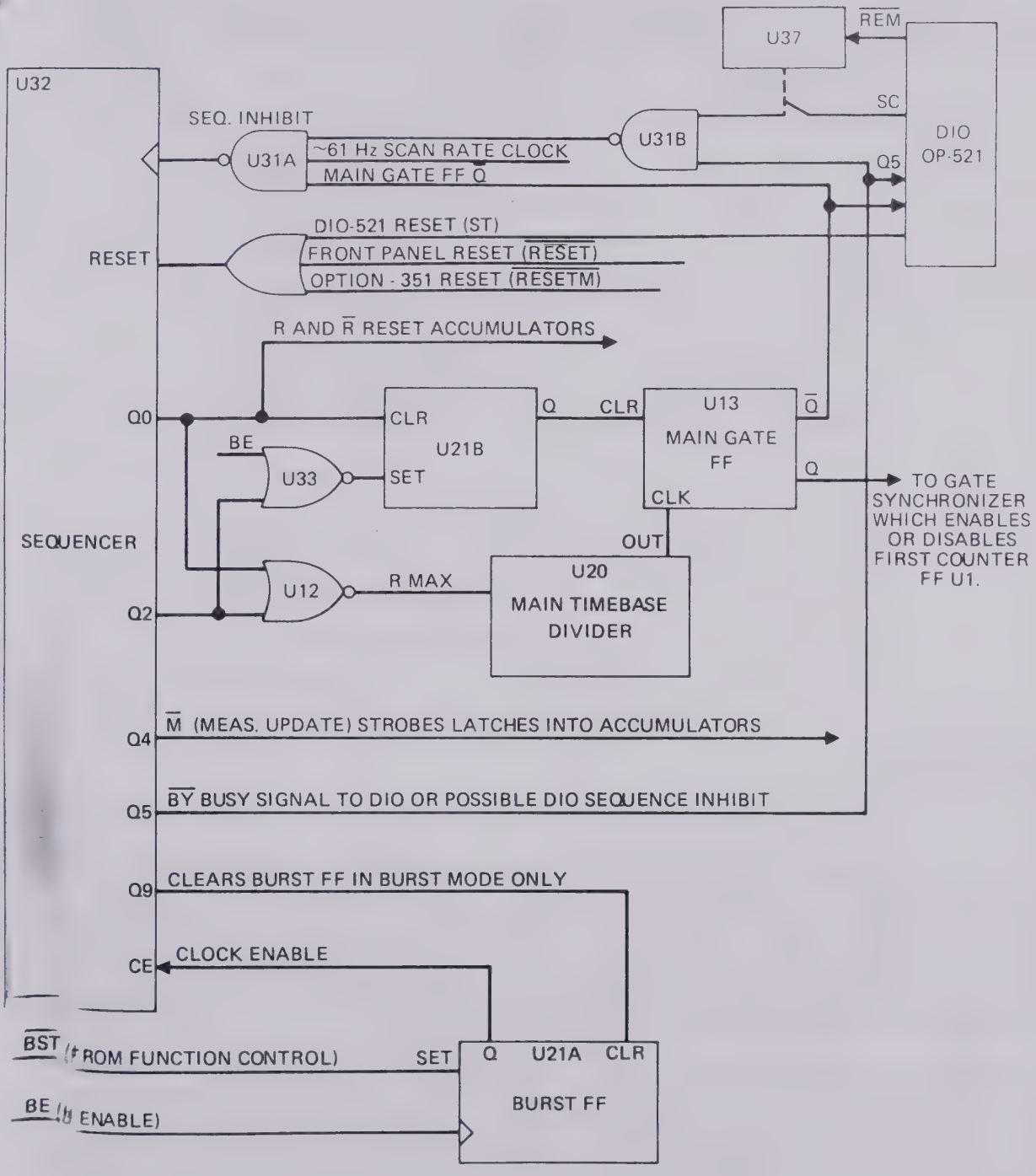


Figure 3-8. 7220A Control Logic

Table 3-2. Sequencer Count Cycle

SEQ. STATE	FUNCTION MODE			
	CHANNEL A	CHANNEL B NON-BURST		CHANNEL B BURST
		with signal above threshold	with signal below threshold	
Q0	Clear Main Gate FF Reset Accumulators Remove U20 R Max (But no gate because Main Gate FF held clear)			
Q1	Nothing happens			
Q2	BE high, so U21B does not set, thus removing U20 R Max, and allowing Main Gate FF to enable U1, beginning gate time. Sequencer inhibited by Main Gate FF $\overline{Q}$ until end of gate time. At end of gate time, Sequencer resumes.		BE low, so U21B sets, which holds Main Gate FF clear and U1 disabled throughout sequence states Q0-Q9.	Same as Channel A
Q3	Nothing happens			
Q4	$\overline{M}$ Measurement Update strobes latches into accumulator, then display		(No measurement, so no display)	
Q5	$\overline{BY}$ Busy signal to DIO Option -521 Also, DIO Remote Sequence Inhibit possible			
Q6-Q8	Nothing happens			
Q9	Nothing happens			Resets BURST FF U21A, which only allows one pass through Q0-Q9.

3-98. A high pulse to R Max will reset U20 counters to all 9's. The counters are held at all 9's as long as R Max is held high. When R Max goes low, or is "released," then the next clock pulse to U20 will advance the U20 counters. As can be seen in Figures 3-7 and 3-8, R Max is released by Q0. This allows the next clock pulse into U20 to advance the counters to all 0's, which generates a pulse on the Out line and clocks the Main Gate FF. However, the Main Gate FF does not respond to the clock signal at this time because it is being held clear by the Q2 output of U32, which is low while Q0 is high. At the next Scan Rate pulse, U32 advances to Q1 which causes U20 to reset to all 9's, but nothing else happens during Q1.

3-99. State Q2

3-100. The First Counter FF can be enabled or disabled during the Q2 state. As shown in Table 3-2, the events that occur during Q2 depend in part on the Function control mode selected. If the Channel B non-BURST mode is selected, the Channel B input signal determines whether or not the gate opens. There are two possible cases. In the first case, if an input signal below threshold is detected by the Threshold Detect Circuit (as described in the section on Channel B signal conditioners), then BE (B Enable) goes low and U21B will set. This will hold the Main Gate FF clear, so that the First Counter FF will not be enabled and no measurement takes place.

3-101. In the second case, if an input signal above threshold is detected by the Threshold Detect Circuit, then BE goes high and U21B will be reset by Q0. As shown in Figure 3-8, Q2 will release R Max. The next clock pulse into U20 turns the counters over to all 0's, generating an Out pulse which clocks the Main Gate FF, U13. This sends U13 $\overline{Q}$ low, inhibiting the Sequencer, and sends U13 Q high, which is presented at the D input to the Gate Synchronizer, U7. The next 100 kHz clock pulse into U7 clocks U7, which enables the First Counter FF, U1, beginning the gate time, and allows the input signal to be counted. U20 counts up to the range selected by the RESOLUTION setting, and again turns over to all 0's,

generating an Out pulse which clocks U13. The Q output of U13 goes low, and is presented at the U7 D input. At the next 100 kHz clock pulse, U7 $\overline{Q}$ goes high and disables the First Counter FF, U1, ending the gate time. Meanwhile, U13 $\overline{Q}$ goes high and removes the Sequence Inhibit, allowing the next 61 Hz pulse to advance the Sequencer to state Q3.

3-102. As shown in Table 3-2, when Channel B BURST and Channel A are selected, the Sequencer follows the same steps as when the Channel B non-BURST is selected and an input signal above threshold is detected. Channel A follows these steps because diode CR7 pulls the $\overline{BE}$ line low, which makes it look like the Channel B non-BURST mode with an input signal above threshold.

3-103. States Q3 and Q4

3-104. Nothing happens in the Q3 state. In the Q4 state, the $\overline{M}$ Measurement Update is generated, which strobes the count into the latches and allows the count to be displayed.

3-105. State Q5

3-106. In the Q5 state, a busy signal is sent to the DIO Option -521 (if installed), which tells the remote interface that a measurement cycle is in progress. As mentioned in the section about the Sequence Inhibit, the Sequencer can also be held in state Q5 by commands from the DIO. Figure 3-8 shows how this works. When the $\overline{REM}$ line is true, the counter's measurement cycle can be controlled by an external controller operating through the -522 and -521 Options (see Section 6) and controlling the SC line.

3-107. When $\overline{REM}$ is low and SC is high, the Sequencer is allowed to go through one measurement cycle beginning at state Q0. When state Q5 occurs and is applied to U31B along with the high SC, the Sequence Inhibit prevents the Scan Rate clock from advancing the Sequencer. The Sequencer remains in state Q5 until a Reset (ST) command is generated through the DIO. When $\overline{REM}$ is low and SC is low, the Sequencer will pass through the measurement cycle continually. This is because the low SC line does not allow the Q5 to remove the Scan Rate clock from the Sequencer. When $\overline{REM}$ is high, the switch U37 grounds the SC line, thus preventing Q5 from inhibiting the Scan Rate clock from the Sequencer. The Sequencer will pass through the measurement cycle continually if not in the BURST mode.

3-108. States Q6 Through Q9

3-109. Nothing happens in states Q6, Q7, and Q8. As mentioned before, when the Channel B BURST mode is selected, state Q9 will reset the BURST FF. This allows only one Q0-Q9 measurement cycle to take place. The Reset command must be generated to allow another measurement cycle to take place in the BURST mode.

3-110. Nine Digit Count and Display

3-111. The 7220A nine digit display capacity is provided by nine decade counters, with appropriate latch, multiplex, driver and display circuitry. Most of the counter, latch and multiplexing capability is provided by U15. As can be seen from Figure 3-9, U15 provides six of the nine decade counters, as well as the latches and multiplexing for the first eight digits. The other three decade counters are external to U15, and the ninth (most significant) digit has its own counter, latch, multiplexer, and control logic to insert the ninth digit information onto the bus lines to the digit and LED segment drivers.

3-112. COUNTERS AND LATCHES

3-113. The counter which supplies the data for the least significant digit is actually composed of four J-K flip-flops. The first Counter FF, U1, a very high speed ECL J-K FF, also serves the gating function for the 7220A. Its clock input is the unknown signal to be measured, and it is enabled or disabled by the Gate Synchronizer, U7, via the J and K inputs. The First Counter FF is also described in the section on Time Base Dividers.

3-114. When the gate signal enables U1, its Q and $\overline{Q}$ outputs pass the divided-by-two signal to the transistor differential pair, Q7 and Q8. Transistors Q7 and Q8 translate the U1 ECL level signal to TTL, and pass it to the next three J-K FF's, which collectively divide the signal by five and provide the rest of the BCD data for the least significant digit. The carry of the last FF passes to the next BCD decade counter which provides BCD data for the second least significant digit. As shown in Figure 3-9, the first two digits of BCD data pass into U15 to be latched. The BCD decade counters for the third through the eighth digits are contained in U15. The carry from the eighth digit counter passes outside U15 to the ninth (most significant) digit BCD counter. When U15 and the ninth digit latch receive the $\overline{M}$ Measurement Update pulse from the Control Logic Sequencer, the eight internal latches of U15 and the ninth digit latch open and receive the BCD data from the counters.

3-115. MULTIPLEXING AND DISPLAY

3-116. The timing for the digit strobing and the LED segment BCD data strobing is outlined in Figure 3-10. During display operation, the Buffer/LED drivers for the nine digits are powered one at a time, beginning with the most significant digit, DS9, on through to the least significant digit, DS1. The multiplexer follows the same sequence to select the proper latch, and presents the BCD data to the BCD-to-Seven-Segment Decoder/Driver,

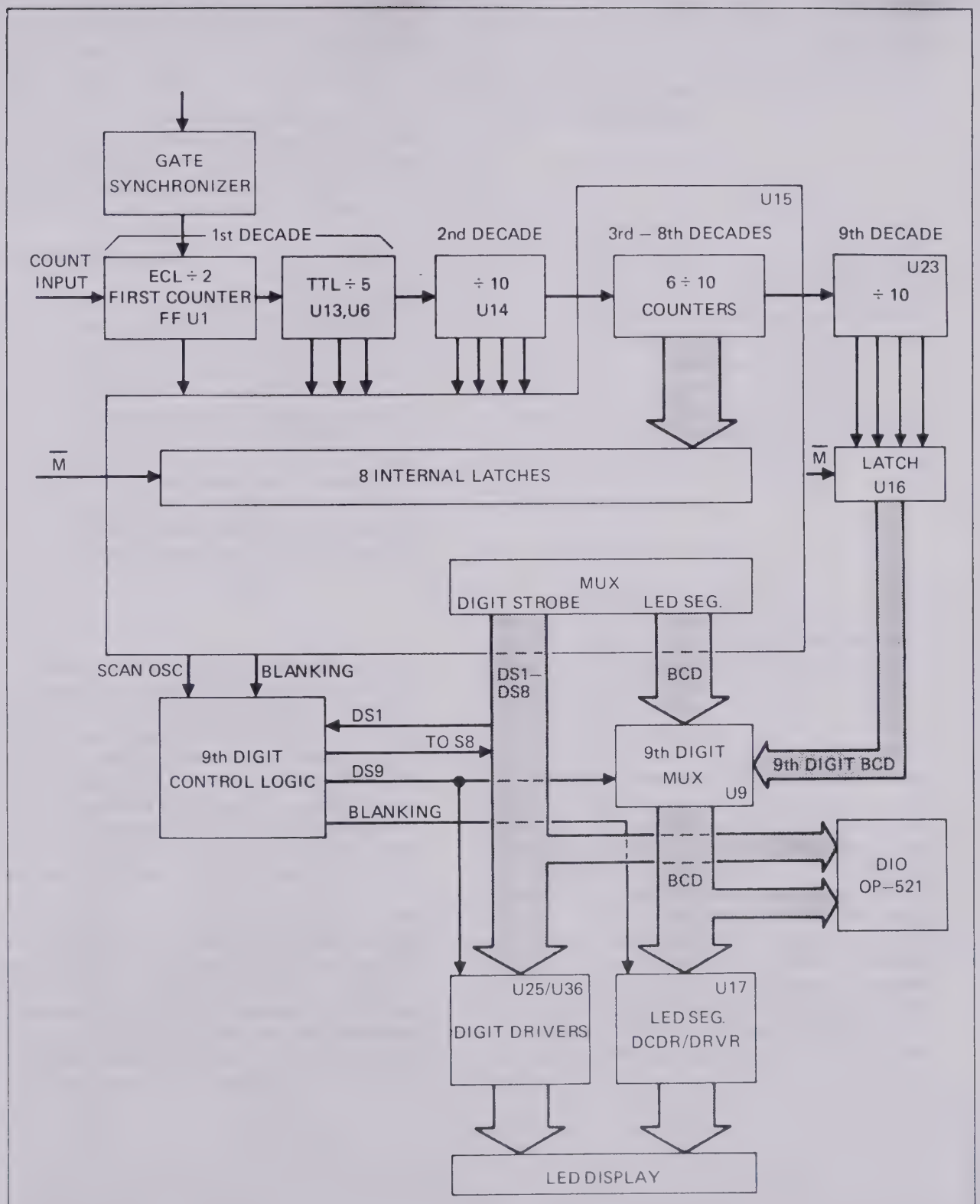


Figure 3-9. Counter and Display Logic

which selects the LED segments required to configure the proper value for that digit to display. The LED segment bus line of the Decoder/Driver is connected to all nine digits in the display, but the only digit that lights up is the one selected and powered at that time by its digit strobe.

3-117. As shown in Figure 3-10, the length of the digit strobe is slightly less than the length of time the BCD data is presented. Both the leading and trailing edge of the data strobe are protected in this way to ensure that the BCD data is displayed by the proper digit strobe.

3-118. U15 Multiplexing

3-119. Multiplexer U15 provides the digit strobing and BCD data multiplexing for digits eight (the second most significant) through one (the least significant). The ninth digit strobing and multiplexing is provided by separate circuitry, and is described later under Ninth Digit Logic. The strobing and multiplexing of U15 is accomplished by an internal scan counter. The scan counter is driven by an internal oscillator whose frequency is determined by the value of capacitor C30 and resistor R61. The oscillator frequency is approximately 1.2 kHz. As can be seen in Figure 3-10, the scan counter advances on the negative edge of the oscillator signal, and it steps through the digits in sequence, from DS8 to DS1.

3-120. Ninth Digit Logic

3-122. The purpose of the Ninth Digit Control Logic, which is shown in Figure 3-11, is to generate the ninth digit strobe (DS9, the most significant digit), and to insert DS9 and the ninth digit BCD data into the U15 scan sequence. The control logic receives input from the oscillator, blanking, and DS1 of U15. At the end of DS1, the control logic generates DS9, and SR, the Scan Reset. DS9 is applied to the Buffer/LED Driver, and also to the Ninth Digit Multiplexer, which routes the BCD data from the ninth digit latch to the LED segment Driver.

3-122. SR forces the Scan Counter of U15 to the eighth digit state, where it is held until SR is released. During SR, the multiplexing function of U15 is held off, although its internal oscillator continues to run. U15 is also held in state DS8, but DS8 is not desired at this time, since DS9 is being strobed. To prevent DS8 from being applied to the Buffer/LED Driver, SR is inverted and tied to DS8 to remove it (in Figure 3-11, S8 is the U15 output at pin 2, while DS8 is the effective digit strobe seen by the Buffer/LED Driver). The Ninth Digit Control Logic holds DS9 and SR for one period of the oscillator, then releases them. Now U15 resumes its scan sequence, beginning with DS8, and continues through the sequence until the completion of DS1, when the Ninth Digit Control Logic again inserts DS9.

3-123. Display Blanking Logic

3-124. The purpose of the Display Blanking Logic is to suppress all but one leading zero occurring in the display. The Display Blanking Logic operation is outlined in Figure 3-12. Flip-flop U35A examines the nine digits from the left (Digit 9, the MSD) to the right (Digit 1, the LSD), and will suppress all but one leading zero. U35A is used as an R-S FF. While it is set, it blanks U17, the LED Segment Driver, and will continue to blank U17 until it is cleared. It is set during DS9 and will be cleared by one of two things: (1) Any non-zero BCD data preceding the decimal point; 2) The BL (blanking) output of U15 if a zero is to precede the decimal point. If a clear input to U35A occurs during DS9, it will override the set input and allow display of DS9.

3-125. Decimal Point Placement

3-126. The purpose of the Decimal Point Placement Logic is to get the decimal point turned on during the proper digit strobe time so it appears in the correct place in the display. Depending on its position, the front panel RESOLUTION switch puts +5V on one of the lines DP1, DP2, DP3, or DP4. U38 is an analog switch which connects any one of these 4 lines (or none of them) to the base of the decimal point driver, Q9. This is shown in Figure 3-13. The digital multiplexer U26 connects one of two possible sets of digit strobes to the control lines of analog switch U38. One combination of digit strobes is connected when using the Resolution Multiplier Option -351, and another is selected when in any of the other Functions, giving the two sets of possible decimal point locations. As digit strobe pulses appear at the analog switch control inputs, C1-C4, the corresponding input DP1-DP4 is connected to the output. When the input line with +5V on it is connected to the output, the decimal point lights in the correct position of the display. Table 3-3 presents a list of Resolution settings and the corresponding Digit Strobes during which the decimal points appear.

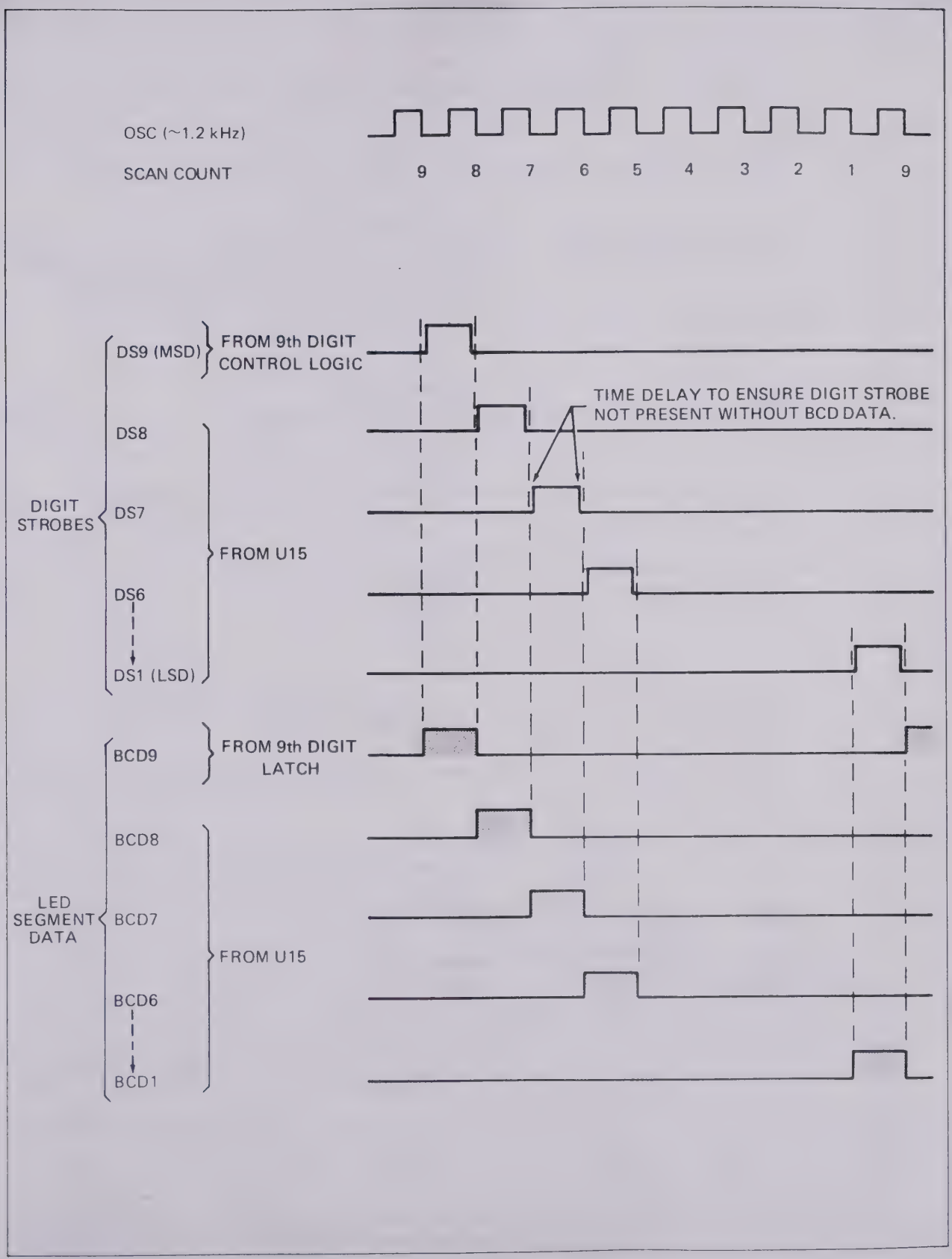


Figure 3-10. Strobing and Multiplex Timing

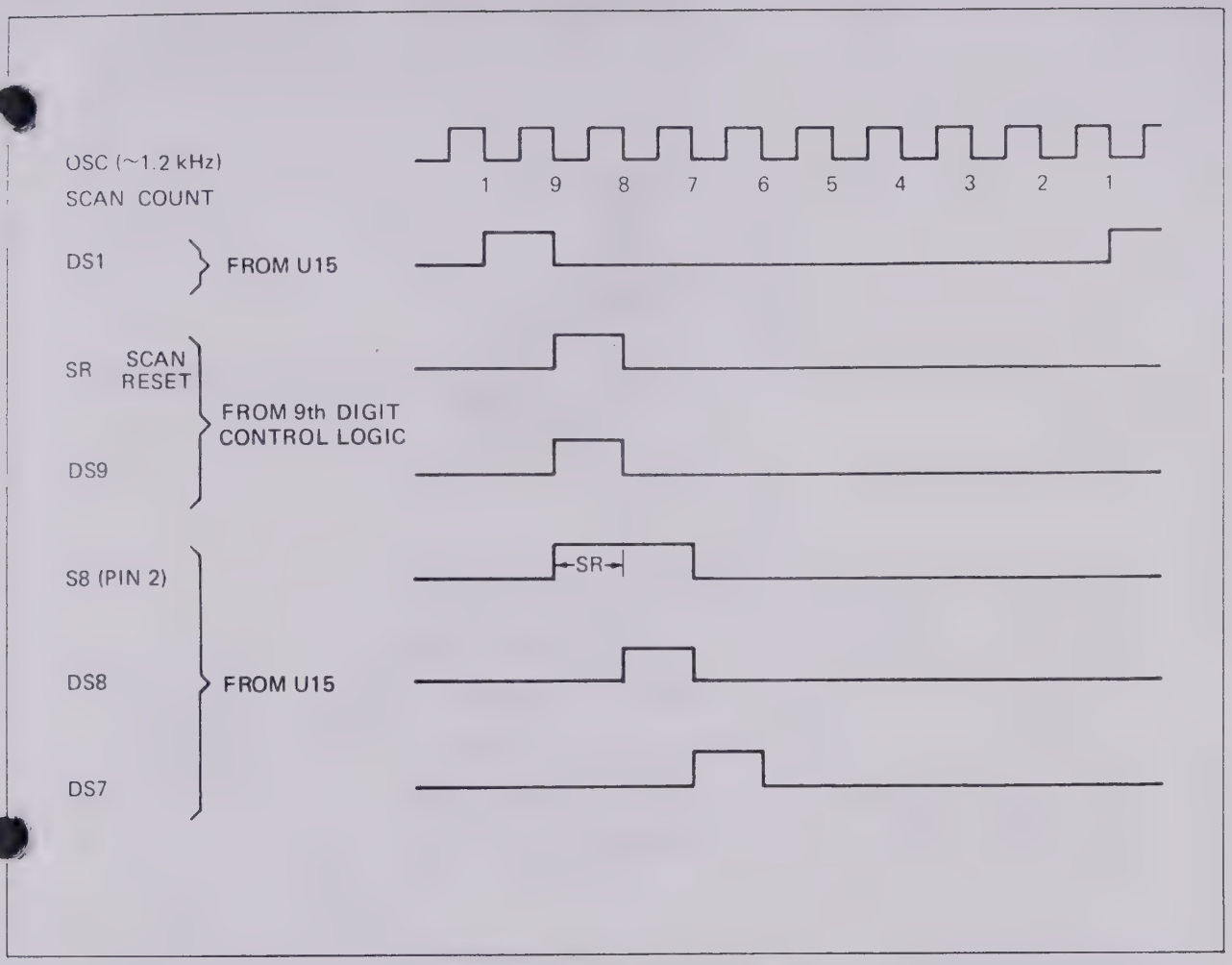


Figure 3-11. Ninth Digit Control Logic

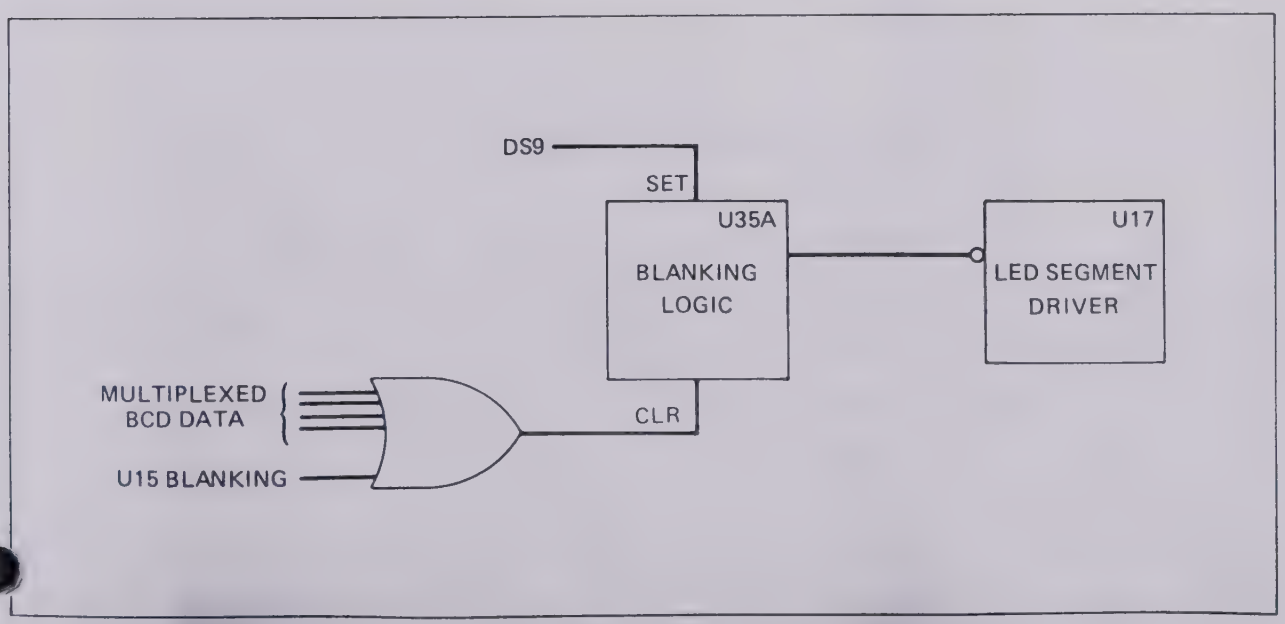


Figure 3-12. Display Blanking Logic

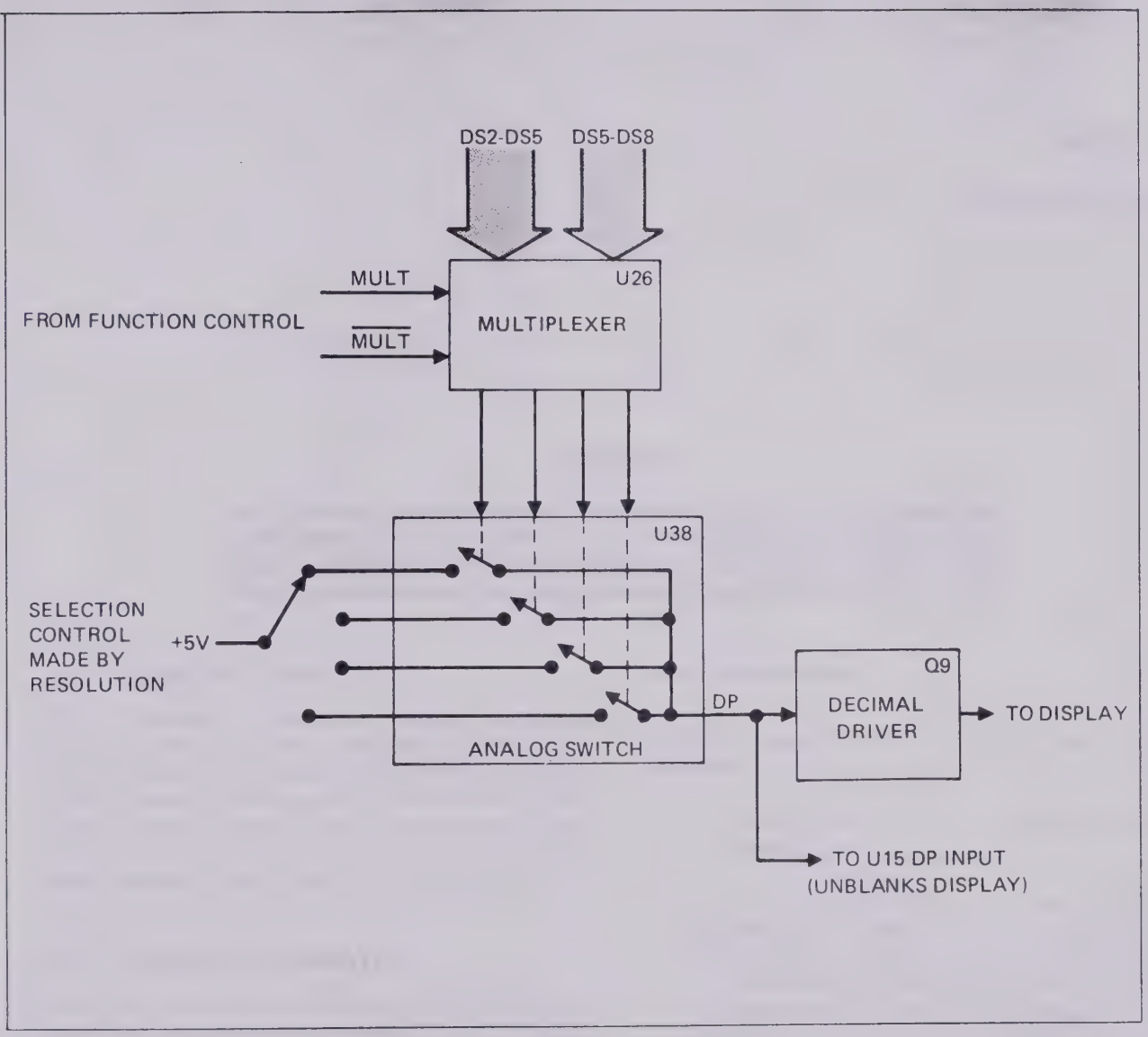


Figure 3-13. Decimal Point Selection

Table 3-3. Decimal Point Digit Strobes

RESOLUTION	DIGIT STROBE	RESOLUTION	DIGIT STROBE
Without Resolution Multiplier MULT = 0 $\overline{\text{MULT}}$ = 1		With Resolution Multiplier MULT = 1 $\overline{\text{MULT}}$ = 0	
100 Hz	DS5	0.1 Hz	DS2
10 Hz	DS6	0.01 Hz	DS3
1 Hz	DS7	0.001 Hz	DS4
0.1 Hz	DS8	0.0001 Hz	DS5

Section 4
Maintenance

WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

4-1. INTRODUCTION

4-2. This section of the manual provides information concerning warranty, general maintenance, performance tests, calibration and troubleshooting for the 7220A Frequency Counter. Test Equipment recommended for performance tests, calibration, and troubleshooting is listed in Table 4-1. If the recommended equipment is not available, equipment with equivalent specifications may be used.

4-3. SERVICE INFORMATION

4-4. The instrument is covered by a warranty for a period of 1 year from the time of delivery to the original purchaser. The WARRANTY is located on the back of the title page of this manual.

4-5. Factory authorized calibration and service for each Fluke product is available at various world wide locations. A complete list of these service centers is included in Section 7 of this manual. If requested, an estimate will be provided to the customer before any work is begun on instruments that are beyond the warranty period.

4-6. GENERAL MAINTENANCE

NOTE

To avoid contaminating the pcbs with oil from the fingers, handle the pcbs by their edges or wear gloves. If a pcb does become contaminated, refer to the cleaning procedure.

4-7. Disassembly

4-8. To disassemble the instrument, use the following procedure:

1. Press the power switch to STBY, and remove the line power cord.

2. On the case bottom, remove the six securing screws. Two of these screws will be found in the middle of the case along the side, under the latches. To access either middle screw, as shown in Figure 4-1, alternately push the two latching rails away from the triangular stop. Pull the latch out far enough to reveal and remove the screws.

NOTE

Do not hold the case bottom while lifting off the case top, as this could result in damage to the Main PCB. The Main PCB is still attached to the case bottom by a screw in the middle of the board.

3. In the front, press down on the BNC input connectors, while gently pulling up on the case top lip. In the rear, press down on the BNC connectors, while pulling up on the top case lip. Alternating between front and back panels, pry the case top free from the rest of the instrument.

Table 4-1. Required Test Equipment

EQUIPMENT TYPE	REQUIRED SPECIFICATIONS	RECOMMENDED TYPE
Oscilloscope	Dual trace, DC-200 MHz wide band	Tektronix 475
High Frequency Signal Generator	1-1300 MHz at a level of 1V rms. Time base 1 x 10^{-8} per day.	HP 8660
Low Frequency Signal Generator	5 Hz-10 MHz at a level of 1V rms. Time base 1 x 10^{-8} per day.	John Fluke 6011A
Variable AC Power Supply	Variable voltage from 0-250V ac.	Variac
Frequency and Time Standard	Aging rate of 5 x 10^{-10} per day or less.	HP 5061A
Digital Multimeter (DMM)	AC volts 0-250V ac. DC volts 0-20V dc with accuracy ±0.1% of reading ±1 digit. Resistance 0 - infinity.	John Fluke 8020A
Variable RF Attenuator	0-50 dB over 0-1500 MHz range.	Weinschel AD-117A
RF Voltmeter	125 MHz, 4 mV rms - 5V rms.	Boonton 92-BD
50 Ohm Terminators (2)	Impedance match the 7220A.	GR 874
BNC Tee		
Oscilloscope Probe	X10, DC-125 MHz	Tektronix P6055

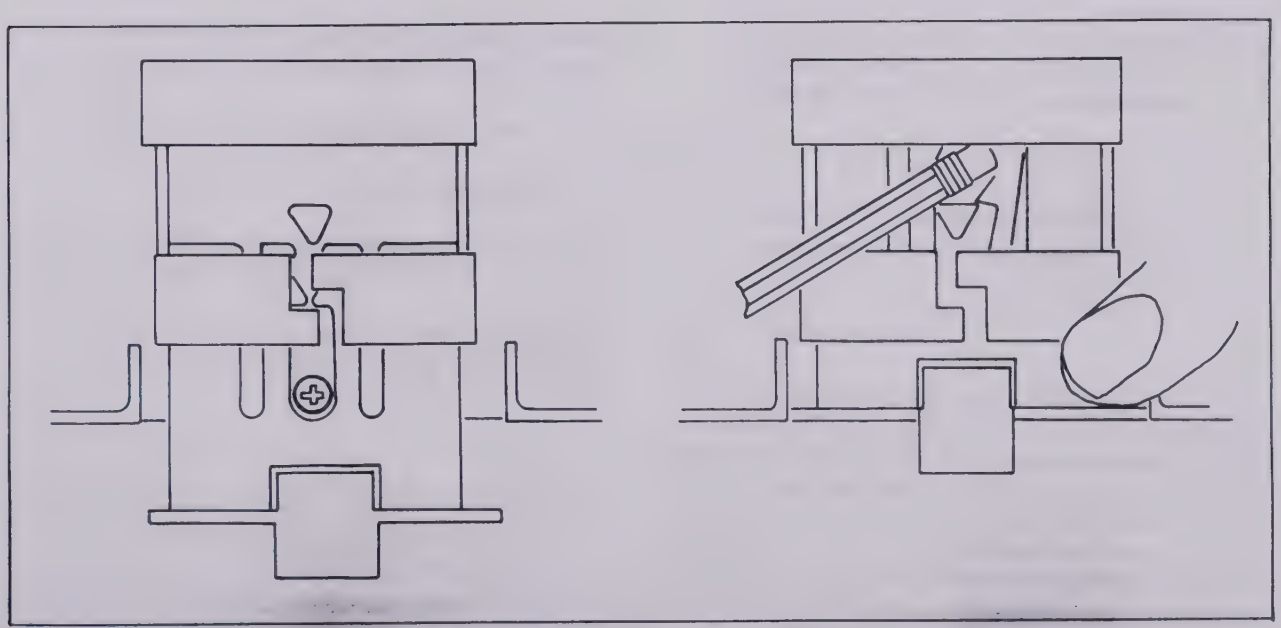


Figure 4-1. Latch Removal

NOTE

For most test and calibration procedures, stop at this step. If continuing beyond this step, take special note of Step 4.

4. Remove the single screw at the middle of the Main PCB, and separate the case bottom.

5. To remove the Front Panel Assembly (A2) from the Main PCB Assembly, first pull off the following switch buttons in the lower left corner of the front panel:

a. ON - STBY (green)

b. BAT - LINE (white)

c. RESET (blue)

6. Gently lift the Front Panel Assembly away from its 40 square-pin connector (left) and guide pin and 3 square pins (right). The Channel B input coax cable may be disconnected from the Main PCB by pulling its connector straight up from the Main PCB.

NOTE

Avoid bending any of the connector square pins on the Main PCB. After removing the Front Panel Assembly, examine the pins and straighten any that are bent before reconnecting the Front Panel Assembly.

7. If it is necessary to separate the Front Panel PCB from the front panel, remove the following items:

a. Front panel Channel A BNC nut.

b. Front panel variable attenuator knob.

c. Mounting screw by the power switch holes (accessible from rear of PCB).

d. Mounting screw by the variable attenuator trimpot R12 (accessible from rear of PCB).

NOTE

When the front panel is separated from the Front Panel PCB, there are no stops to prevent the slide switch actuators from moving beyond their proper position. Care must be taken to keep them in position.

8. To remove the rear panel, first remove the top and bottom case covers. If the Option -521 PCB has been installed, it must be detached from its Main PCB connector before the rear panel can be removed. Remove the two rear panel mounting screws that attach the heat sink to the Main PCB (see Figure 4-8). Carefully pull the bottom of the rear panel outward so it can clear the REF switch, and firmly pull the rear panel straight up, pulling the leads of the 3 regulators (U40, U41 and U42) out of their sockets.

9. Refer to Section 6 of this manual when removing any optional assemblies.

4-9. Reassembly

4-10. For reassembly, the disassembly procedures can generally be followed in reverse order. Keep the following considerations in mind:

1. When reinstalling the Front Panel Assembly, care should be taken not to bend the connector square pins, and to align the three square pins on the right side so they correctly engage their sockets.

2. When reinstalling the rear panel, care should be taken not to bend the regulator leads. Also, be sure to firmly tighten the mounting screws that connect the heat sink to the Main PCB. The regulator leads will not be firmly seated unless these screws are firmly tightened.

3. When reconnecting the top and bottom case halves, ensure that the Front and Rear Panels fit into their appropriate grooves in the case top half. Slide the top half into place uniformly. Firmly squeeze top and bottom together (at front and rear), and reinstall the six securing screws.

NOTE

Proper RFI shielding depends on top and bottom case halves being securely mated.

4-11. Input Power

4-12. Input line voltage is selected by positioning the two switches in the right rear corner of the Main PCB. Each switch (S4 and S5) shows a position identifying red or white dot. Line voltage settings identified by dot color are presented in Figure 4-7. Factory line voltage settings of 100V, 120V, 220V, or 240V are identified on the rear panel of the instrument. When changing the line voltage, refer to the Power Supply Adjustment under the Calibration Adjustments section.

4-13. Fuse Replacement

WARNING

BEFORE ATTEMPTING FUSE REPLACEMENT, REMOVE LINE POWER FROM THE INSTRUMENT.

4-14. The 7220A line power fuse F1 is accessible on the rear panel, and fuse requirements are marked on the rear panel beside the fuse holder. A 1/4A (slo-blo MDL Fluke #166306) fuse is required for line inputs of 100V or 120V, and a 1/8A (slo-blo MDL Fluke #166488) fuse is required for line inputs of 220V or 240V. If fuse replacement is necessary, disconnect the 7220A from line power and remove the fuse cap and fuse (twist the fuse cap ccw using a screwdriver), and replace the fuse.

4-15. The Channel B input is fuse-protected by fuse F2, a 2/10A plug-in fuse (Fluke #370577) which is plugged into the Main PCB next to the Channel B coaxial cable. There is also a spare Channel B fuse, F3, which is plugged into the Main PCB in front of the transformer T1. Both of these fuse locations can be seen in Figure 4-8. To remove F2 or F3, remove the top and bottom case halves from the Main PCB. Firmly work the fuse straight out from its socket.

4-16. Cleaning

4-17. Clean the instrument periodically to remove dust, grease and other contamination. Use the following procedure:

CAUTION

Do not use aromatic hydrocarbons or chlorinated solvents for cleaning. They will react adversely with plastic materials used in manufacture of the instrument.

1. Clean the front panel and case with soft cloth dampened with a mild solution of detergent and water.

2. Clean the surface of the PCBs using clean, dry air at low pressure (=20 psi). If grease is encountered, spray with Freon T.F. Degreaser or anhydrous alcohol and remove grime with clean, dry air at low pressure.

4-18. PERFORMANCE CHECKS

4-19. The Performance Checks are used to compare the performance of the instrument with the Specifications given in Section 1. The Performance Checks are recommended as an acceptance test when the unit is first received, and later as a calibration procedure to verify instrument accuracy at the scheduled calibration periods. It is also useful as an aid in troubleshooting. All of the Performance Checks other than the Time Base Check should be performed every 90 days. The Time Base Check should be performed as often as the desired Specification requires. Should the instrument fail any portion of the Performance Checks, calibration and/or repair may be needed. Refer to Table 4-1 when specific test equipment is required.

4-20. Initial Set-up

4-21. The following controls should be in the indicated positions prior to conducting any Performance Check.

1. On the rear panel of the 7220A, set the REF to INT. The line power cord should be connected to line power.

2. On the front panel of the 7220A, set the controls as follows:

ON/STBY	ON
BAT/LINE	LINE
RESOLUTION	10 Hz
CH A/CH B	CHK
VAR. ATTENUATION	Fully CCW
STEP ATTENUATION	X1

3. Set CH A/CH B to CHK. Verify the display as listed in Table 4-2.

4. Observe that the display resets each time the RESOLUTION or CH A/CH B switches are changed.

To verify the operation of the RESOLUTION MULTIPLIER mode, see the Performance Check in Section 6.

Table 4-2. Display Check

FUNCTION	RESOLUTION	DIGIT DISPLAY
125 MHz	100 Hz	0.0000
125 MHz	10 Hz	0.00000
125 MHz	1 Hz	0.000000
125 MHz	0.1 Hz	0.0000000
CHK	100 Hz	10.0000
CHK	10 Hz	10.00000
CHK	1 Hz	10.000000
CHK	0.1 Hz	10.0000000

4-22. Time Base and Time Base Output Check

4-23. Use the following procedure to check the accuracy of the time base and the operation of the INT REF OUT circuitry:

NOTE

To check the time base, the source of the input signal must have an accuracy greater than that of the time base. Refer to Table 4-3 for the maximum allowable time base error, and refer to Table 4-1 for the recommended Frequency and Time Standard.

1. Set the 7220A controls as listed in the Initial Set-up except for the following changes.

RESOLUTION	0.1 Hz
CH A/CH B	125 MHz

2. Connect a 10 MHz Frequency standard to the Channel A input terminal.

3. Verify that the display reading on the 7220A is 10 MHz ± the maximum allowable count error. Table 4-3 lists the maximum allowable count error at 10 MHz (and 0.1 Hz resolution) for each of the four time bases available for use with the instrument. The maximum allowable count error can be computed for any input signal by multiplying the frequency of the input signal by the total time base accuracy (given in Table 4-3) and adding the ±1 count error to the product.

4. Connect the oscilloscope to the REF OUT terminal on the 7220A rear panel through as short a length of RG-58 cable as possible. The oscilloscope end of the test cable must have a 50 ohm termination. Be sure the 7220A rear panel REF is set to INT.

5. Verify that the signal displayed on the oscilloscope is 10 MHz.

4-24. Channel A Input Sensitivity Check

4-25. Use the following procedure to verify that Channel A input sensitivity lies within the Specifications given in Section 1:

1. Set the 7220A controls as listed under Initial Set-up except for the following changes:

Rear panel:	REF	EXT
Front panel:	CH A/CH B	125 MHz

2. Connect the 7220A and test equipment as illustrated in Figure 4-2.

3. Verify that correct readings are displayed for the input signals and voltage levels listed in Table 4-4.

NOTE

The stability of counter readings will be no greater than the stability of the Signal Generator.

4. Set the 7220A RESOLUTION to 0.1 Hz. Apply a Channel A input signal of 125 MHz at 100 mV rms. Following a 10 second gate time, verify that the display is 25 MHz and that the OVFL LED is lit. 100mV = 282.8mV pk-pk

Table 4-3. Time Base Performance Check

TIME BASE TYPE	FREE AIR	1 PPM TCXO OPTION -111	OVEN OPTION -131	OVEN OPTION -132
Total Time Base Accuracy*	$\pm 56 \times 10^{-7}$	$\pm 15.0 \times 10^{-7}$	$\pm 2.2 \times 10^{-7}$	$\pm 8.4 \times 10^{-8}$
Maximum Allowable Deviation** (with 10 MHz input)	±56.1 Hz	±15.1 Hz	±2.3 Hz	±0.9 Hz

**Includes aging rate per month, temperature effects, line voltage variation.*

***Allowable deviation in Hz is found by multiplying the input frequency (10 MHz in this case) by the total accuracy, and adding 1 count error. These figures apply when in 0.1 Hz resolution.*

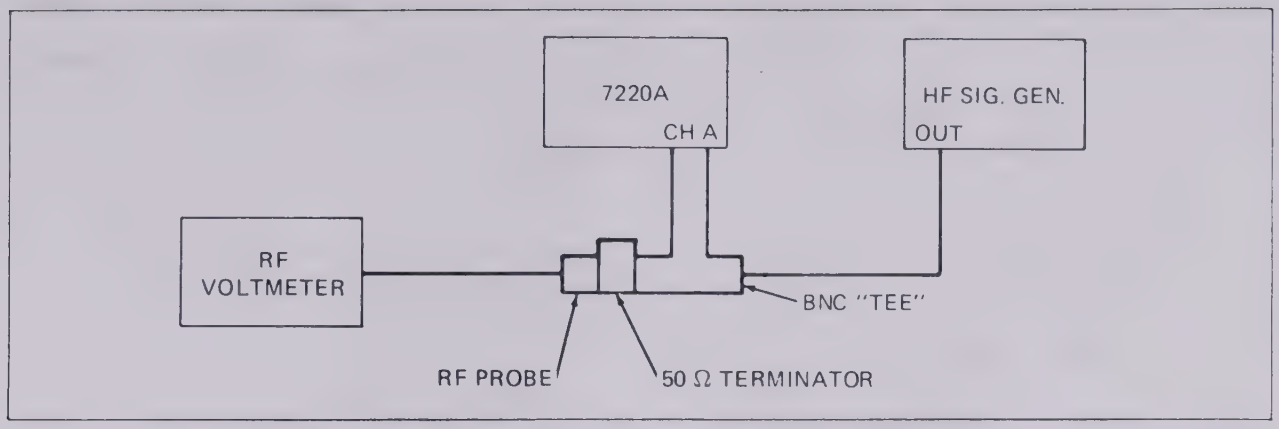


Figure 4-2. Channel A High Frequency Input Sensitivity Check

Table 4-4. Channel A High Frequency Input Sensitivity

INPUT SIGNAL	VOLTAGE (rms)
50 MHz	10 mV 28.28pk-pk
100 MHz	15 mV 42.42pk-pk
125 MHz	25 mV 70.71pk-pk

5. Set the 7220A RESOLUTION to 10 Hz. Apply a Channel A input signal of 125 MHz at 25 mV rms. While varying the input signal voltage level from 25 mV rms to 1 V rms, observe a correct display of 125 MHz at all voltage levels. 1Vrms = 2.828v pk-pk

6. Disconnect the High Frequency Signal Generator and RF voltmeter from the 7220A, and connect the Low Frequency Signal Generator as shown in Figure 4-3.

7. Verify that correct readings are displayed for the 7220A RESOLUTION settings, input signals and voltage levels listed in Table 4-5.

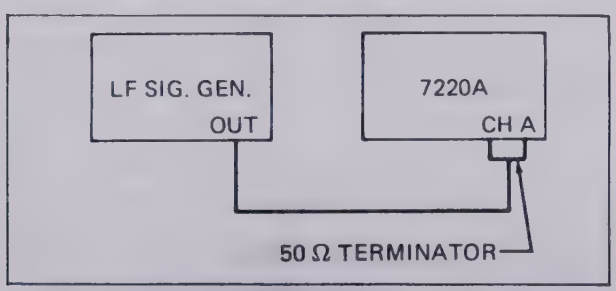


Figure 4-3. Channel A Low Frequency, Filter, and Attenulation Check

Table 4-5. Channel A Low Frequency Input Sensitivity

RESOLUTION	INPUT SIGNAL	VOLTAGE (rms)
1 Hz	10 Hz	10 mV
1 Hz	1000 Hz	10 mV
10 Hz	50 kHz	10 mV
10 Hz	1 MHz	10 mV
10 Hz	10 MHz	10 mV

10mV = 28.28mV

4-26. Channel A Filter Check

4-27. Use the following procedure to verify that the Channel A 100 kHz low pass filter operates properly:

1. Set 7220A controls as listed under Initial Set-up except for the following changes:

RESOLUTION	1 Hz
CH A/CH B	125 MHz

2. Connect the 7220A and test equipment as illustrated in Figure 4-3.

3. Apply a 1 MHz signal at 10 mV to the Channel A input.

4. Set CH A/CH B to FILT .1 MHz. Observe that the display reads 0.000000 MHz with the input signal voltage level the same as in Step 3.

5. Gradually increase the input signal level until the 7220A again correctly displays 1.000000 MHz (± time base error ±1 count). Verify that the input signal voltage level is 33 mV to 61 mV.

4-28. Attenuation Check

4-29. Use the following procedure to verify proper operation of the 7220A variable and step attenuators:

1. Connect the 7220A and test equipment as illustrated in Figure 4-3.

2. Set the 7220A controls as listed under the Initial Set-up except for CH A/CH B which should be set to 125 MHz. Be sure the attenuators are set as follows:

VAR. ATTENUATION	Fully CCW
STEP ATTENUATION	X1

3. Apply a 1 MHz signal to the Channel A input at 10 mV. Verify that the display is 1 MHz.

4. Change the STEP ATTENUATION to X10. Verify that the display goes to 0.00000 MHz.

5. Change the input signal level to 100 mV. Verify that the display is 1 MHz.

6. Change the VARIABLE ATTENUATION to fully CW. Verify that the display goes to 0.00000 MHz.

7. Change the input signal level to 1V. Verify that the display is 1 MHz.

4-30. Channel B Operation and BURST Check

4-31. Use the following procedure to verify that the Channel B non-BURST and BURST modes operate properly:

NOTE

All signal levels in this section are actual levels. Attenuator settings may be different depending on the calibration of the High Frequency Signal Generator output level.

1. Connect the 7220A and test equipment as illustrated in Figure 4-4. Set 7220A controls as listed under Initial Set-up except for the following changes:

Rear panel REF	INT
Front panel CH A/CH B	1300 MHz

2. Set the High Frequency Signal Generator to 600 MHz with 0 dBm output, and set the attenuator to 35 dB. Verify that the 7220A displays 600 MHz.

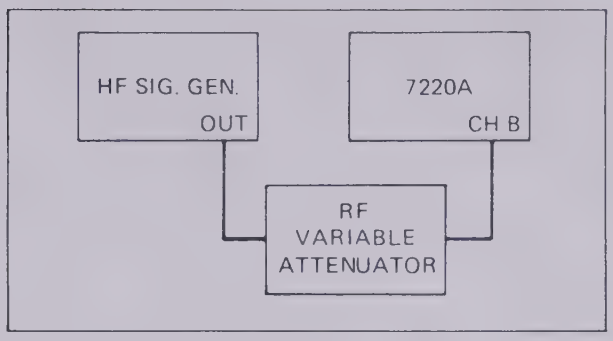


Figure 4-4. Channel B Check

3. Set the attenuator to 41 dB. Verify that the GATE LED turns off and that the display is 0.00000 MHz.

4. Set the CH A/CH B switch to 1300 BURST. Set the High Frequency Signal Generator to 800 MHz with 0 dBm output, and set the attenuator to 42 dB.

5. Press and then release the 7220A front panel RESET switch. Verify a display of 0.00000 MHz and that the GATE LED is not flashing.

6. Set the attenuator to 32 dB. Verify that the 7220A gates once and only once, resulting in a display of 800 MHz.

7. Remove the attenuator and connect the High Frequency Signal Generator directly to the Channel B input. Set the CH A/CH B switch to 1300 MHz.

8. Verify that correct readings are obtained at the input signal frequencies and voltage levels listed in Table 4-6.

Table 4-6. Channel B Input Signals

INPUT SIGNAL	INPUT VOLTAGE
50 MHz	5 mV
600 MHz	5 mV
1000 MHz	10 mV
1300 MHz	40 mV

4-32. External Clock Input Check

4-33. Use the following procedure to verify proper operation of the 7220A rear panel External Clock input.

1. Set the 7220A controls as listed under the Initial Set-up except for the rear panel REF switch, which should be set to EXT.

2. Press and release the front panel RESET and verify the counter reads 0.00000 MHz.

3. Connect the Low Frequency Signal Generator to the 7220A rear panel 10 MHz REF IN input as indicated in Figure 4-5 (the 50 ohm terminator must be connected as shown).

4. Apply a 10 MHz 300 mV signal from the Low Frequency Signal Generator, and verify that the 7220A is gating and the display is 10 MHz.

5. Set the 7220A rear panel REF switch to INT and verify the 7220A is gating and the display is 10 MHz.

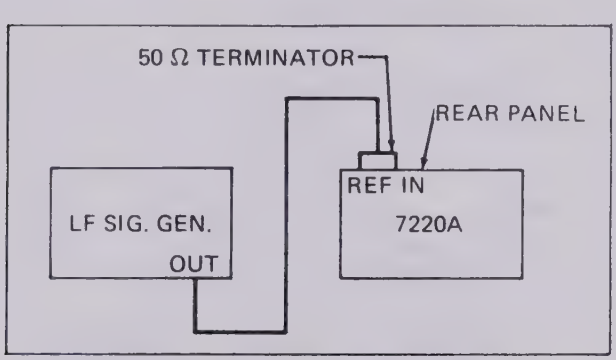


Figure 4-5. External Clock Input Check

4-34. Crosstalk Check

4-35. Use the following procedure to verify that there is no signal crosstalk under normal operating conditions.

1. Connect the 7220A and test equipment as illustrated in Figure 4-6.

2. Set the 7220A controls as listed under the Initial Set-up except for CH A/CH B which should be set to 125 MHz.

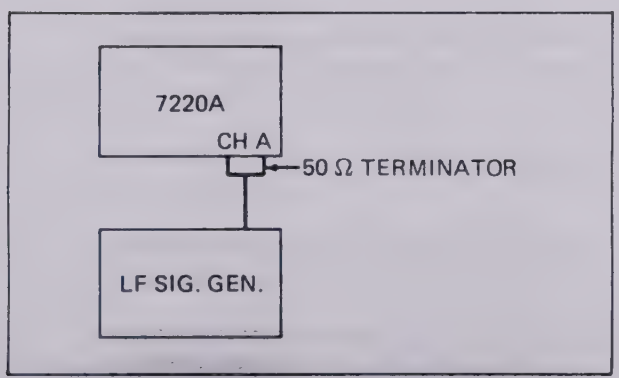


Figure 4-6. Crosstalk Check

3. Apply a 5 MHz 100 mV rms input signal to Channel A. Observe a display of 5 MHz.

4. Set the CH A/CH B to CHK. Observe the display for at least 30 seconds and verify that there is never a reading other than 10.00000 MHz (± time base error ±1 count).

4-36. CALIBRATION ADJUSTMENTS

4-37. These procedures should be performed whenever the instrument has been repaired or fails to pass the Performance Checks. Refer to Table 4-1 when test equipment is required. Unless otherwise specified, refer to the disassembly instructions in the General Maintenance section and remove the top half of the instrument case.

4-38. Power Supply Adjustment

4-39. Use the following procedure to adjust the regulated +5V power supply, to check the regulated +5V, +12V, and -12V power supplies, and to adjust and check the Channel B 6.8V tracking regulator. This procedure should be followed after replacement or repair of the power supply. Line voltage selection of 100V, 120V, 220V, or 240V is provided by switches S4 and S5. S4 and S5 are located on the right rear of the Main PCB, and their position is indicated by a red or white dot. Line voltage selection and the corresponding switch configuration is illustrated in Figure 4-7.

NOTE

See Figure 4-8 for location of test points and trimpots referred to in this procedure.

1. At the ac input receptacle of the 7220A, use the DMM to measure the resistance between the ground pin (center pin) and the chassis. The resistance should be less than 0.1 ohm.

2. Use the DMM to measure the resistance between the two 7220A line voltage pins and the chassis. The resistance should be infinite.

3. Set the variable transformer to 0V and connect to line power. Connect the 7220A line power cord to the variable transformer.

4. Set the 7220A controls as follows:

Rear panel REF	INT
Front panel ON/STBY	ON
BAT/LINE	LINE

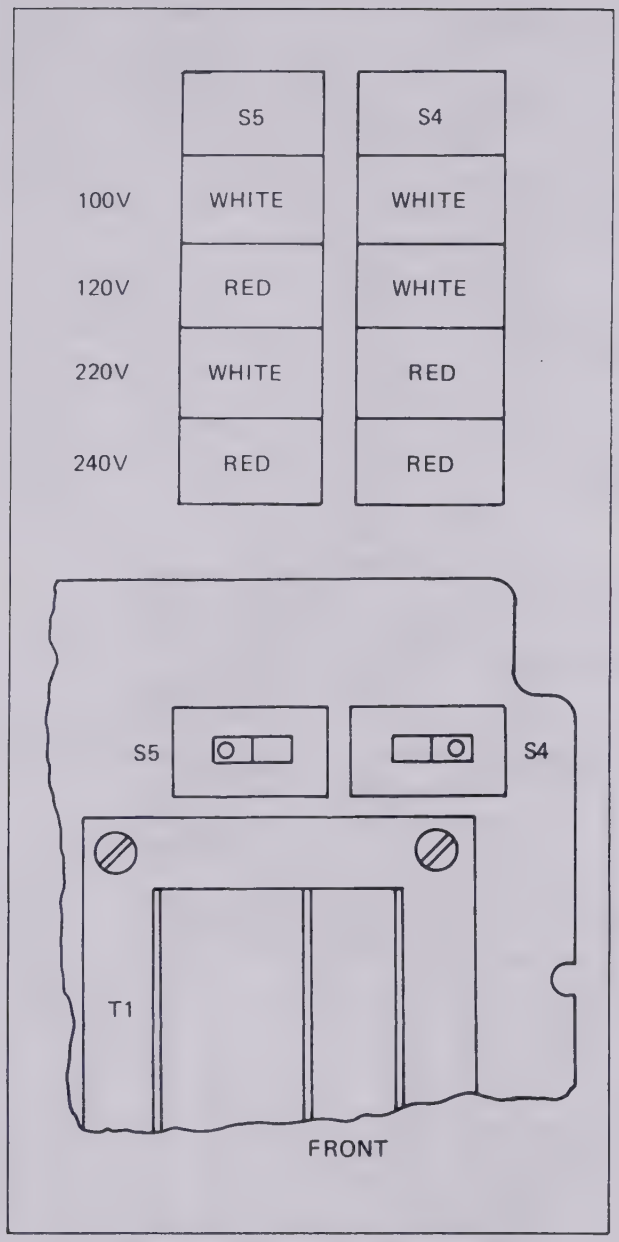


Figure 4-7. Line Voltage Selection

5. Refer to the voltage selection guide in Figure 4-7 and position S4 and S5 to select the line voltage at which the 7220A is to be operated.

6. Slowly raise the variable transformer voltage to the line voltage selected.

7. Connect the DMM positive lead to TP3, and the negative lead to E1 (or any other common ground).

8. While observing the DMM display, adjust R69 to obtain 5.00 ±.01V dc. This adjusts the +5V regulated power supply.

9. Using the DMM and an ac coupled oscilloscope, check the power supply outputs for the tolerance ranges and maximum ripple voltages as given in Table 4-7. In each case the DMM positive lead and the oscilloscope probe should be connected to the test points listed, and the negative lead connected to E1 (or any other common ground).

10. Lower the variable transformer voltage to the selected line voltage minus 10% (for example, if the line voltage selected in Step 5 was 120V, now lower the variable transformer voltage to 108V).

11. Repeat Step 9.

12. Raise the variable transformer voltage to the line voltage selected in Step 5 plus 10%.

13. Repeat Step 9.

NOTE

Steps 5 through 13 may be performed to adjust the +5V regulated power supply and to check the power supplies for any line voltage selected. Before changing the positions of S4 and S5, be sure to reduce the variable transformer voltage to 0V.

14. Be sure S4 and S5 are in the proper position, and return the variable transformer voltage to the line voltage selected.

15. Set the 7220A CH A/CH B control to 1300 MHz. Connect the DMM positive lead to TP8 and the negative lead to TP9.

16. While observing the DMM display, adjust R14 to obtain 6.80 ± .05V dc. This adjusts the Channel B 6.8V tracking regulator.

17. Set the 7220A CH A/CH B control to 125 MHz. Use the DMM to verify that the voltage between TP8 and TP9 is now 0.2 + 0.1V dc.

Table 4-7. Power Supply Levels

TESTPOINT	SUPPLY	TOLERANCE	MAXIMUM RIPPLE
TP3	+5V	±0.01V	50 mV p-p
TP1	+12V	±0.5V	50 mV p-p
TP2	-12V	±0.5V	50 mV p-p

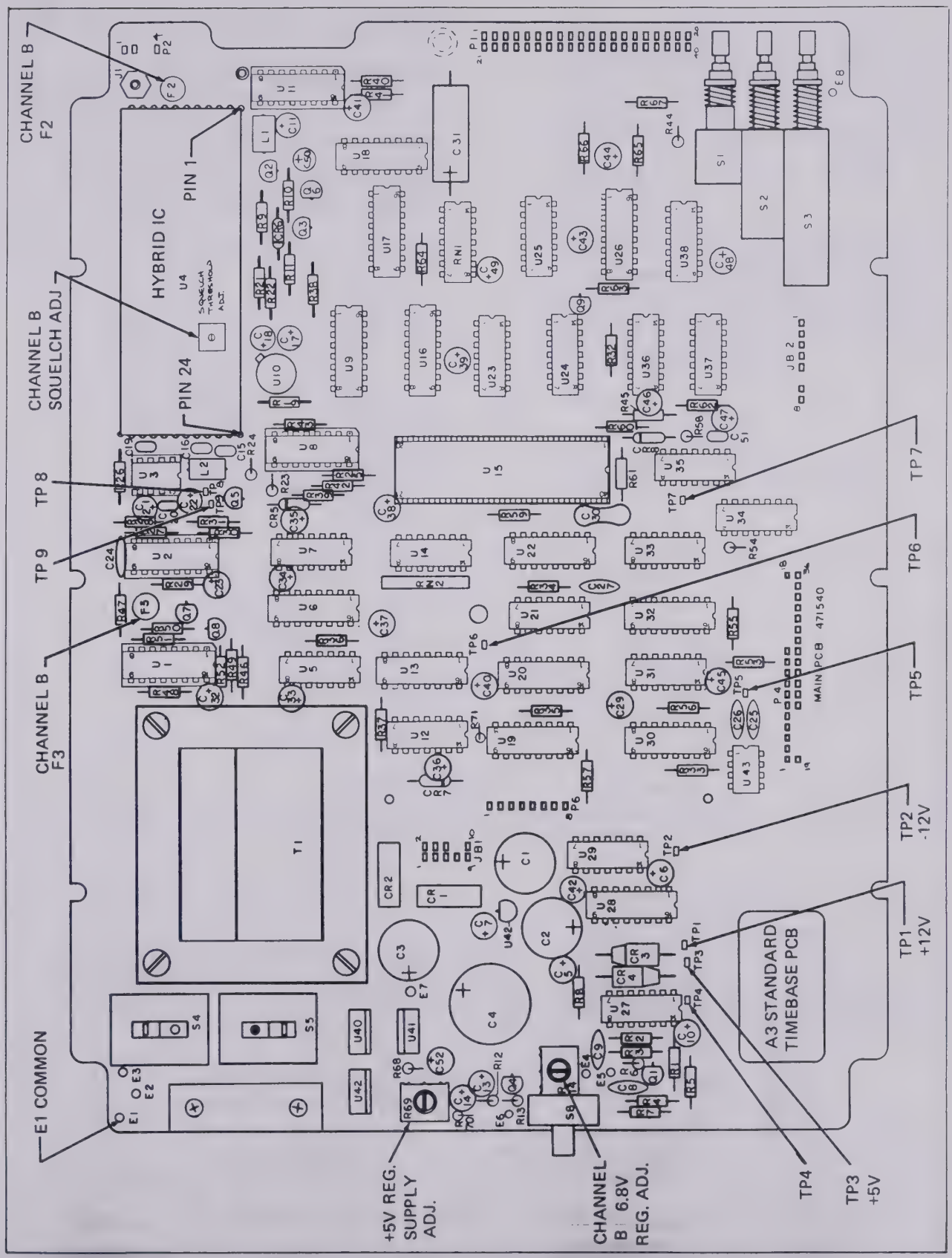


Figure 4-8. Main PCB Testpoint and Adjustment Location

4-40. Channel A Trigger Level Adjustment

4-41. Use the following procedure to adjust the Channel A Trigger Level Adjustment:

1. Using appropriate BNC adapters, connect the Low Frequency Signal Generator and the rf voltmeter with a 50 ohm terminator to the Channel A input of the 7220A. This is illustrated in Figure 4-9.

2. Set the 7220A controls as follows:

Rear panel	
REF	INT
Front panel	
ON/STBY	ON
BAT/LINE	LINE
RESOLUTION	10 Hz
CH A/CH B	125 MHz
VAR. ATTENUATOR	Fully CCW
STEP ATTENUATOR	X1

3. Apply 1 MHz at 10 mV rms to Channel A. Adjust R10 Trigger Adjust trimpot (located on the top of A2, the Front Panel PCB; see Figure 4-10) if necessary to obtain a reading of 1.00000 MHz (± time base error ±1 count). Reduce input voltage level and continue to adjust R10 to obtain the correct display, but do not reduce the voltage level below 4.7 mV rms.

4. If R10 cannot be adjusted to obtain the correct reading at the 4.7 mV rms input level, adjust it midway between fully CW and fully CCW. Turn the R11 Hysteresis Adjust trimpot (located on the right rear of A2, the Front Panel PCB; see Figure 4-10) fully CW. Then slowly turn R11 CCW until the correct reading is displayed.

NOTE

Do not turn R11 CCW beyond the point where the correct reading is first displayed.

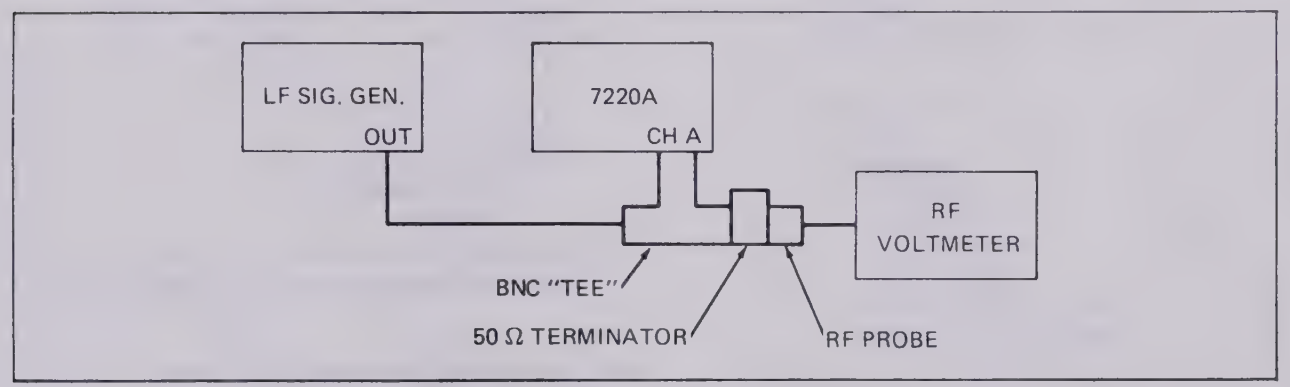


Figure 4-9. Channel A Trigger Level Adjustment

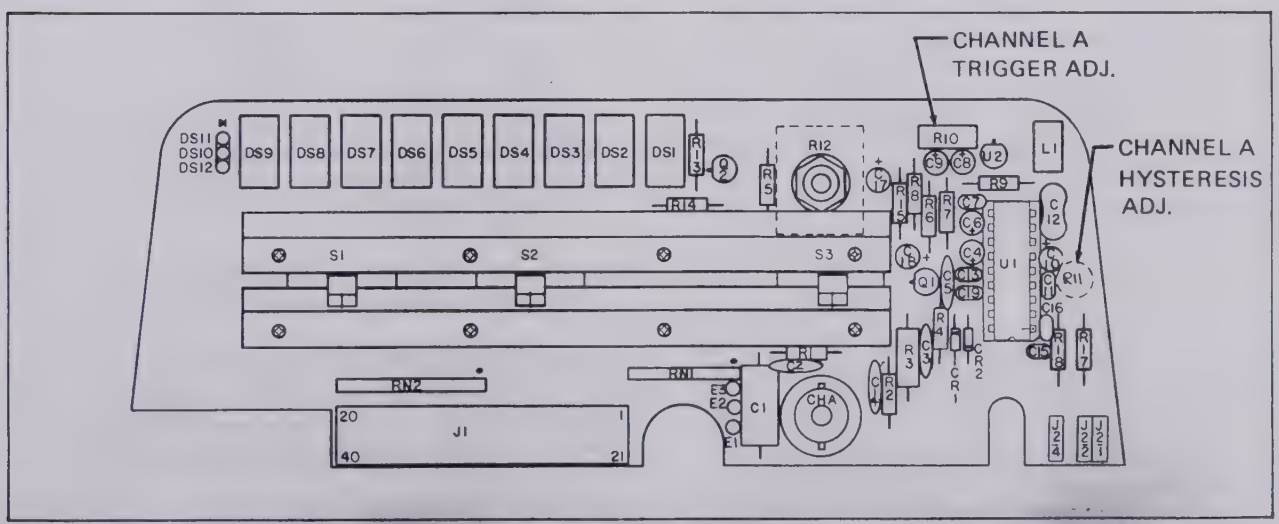


Figure 4-10. Front Panel PCB Adjustment Location

5. Recheck R10 as in Step 3.

6. Recheck R11 as in Step 4.

7. Decrease the input voltage level to 4.25 mV rms. Verify that the 7220A displays unstable, fluctuating readings less than 1.00000 MHz. If the display still indicates 1.00000 MHz (± time base error ±1 count), repeat Steps 4-6.

4-42. Channel B Squelch Adjustment

4-43. Use the following procedure for the Channel B Squelch Adjustment:

1. Connect the 7220A and test equipment as indicated in Figure 4-11.

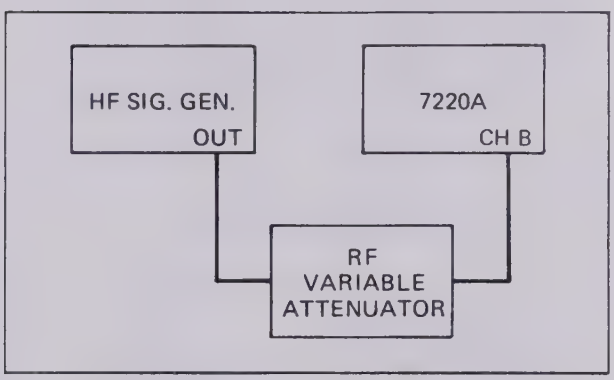


Figure 4-11. Channel B Squelch Adjustment

2. Set the 7220A controls and indicators as follows:

Rear panel	
REF	INT
Front panel	
ON/STBY	ON
BAT/LINE	LINE
RESOLUTION	10 Hz
CH A/CH B	1300 MHz
VAR. ATTENUATOR	Fully CCW
STEP ATTENUATOR	X1

3. Set the High Frequency Signal Generator to 600 MHz at 0 dBm, and the attenuator to 39 dB.

4. Turn the Squelch Adjust trimpot (located on the Channel B hybrid IC, U4; see Figure 4-8) fully CCW. Then adjust the R51 trimpot CW until the 7220A displays 600 MHz.

5. Change the attenuator to 41 dB. Verify that the GATE LED turns off and that the display is 0.00000 MHz. If the 7220A still displays 600 MHz, repeat Steps 4 and 5 until the 7220A displays 60(MHz at 39 dB attenuation, and 0.00000 MHz at 4 dB attenuation.

4-44. Standard Time Base Calibration

4-45. Calibration should be made whenever the tim base is repaired or replaced, or when it is determined tha the instrument accuracy is not within the Specification given in Section 1. The following procedure is to be use(for calibration of a standard time base. Calibratio procedures for any of the optional time bases (Option -111, -131, or -132) are provided in Section 6. The calibra tion should be performed in an environment having a ambient temperature between 20° and 30° C (68° an 86° F).

NOTE

The 7220A must be operating for at least thirty minutes with top and bottom covers on before this procedure is followed.

1. Set the 7220A controls as follows:

Rear panel	
REF	INT
Front panel	
ON/STBY	ON
BAT/LINE	LINE
RESOLUTION	1 Hz
CH A/CH B	125 MHz
VAR. ATTENUATION	Fully CCW
STEP ATTENUATION	X1

2. Connect the 7220A and test equipment as illustrated in Figure 4-12.

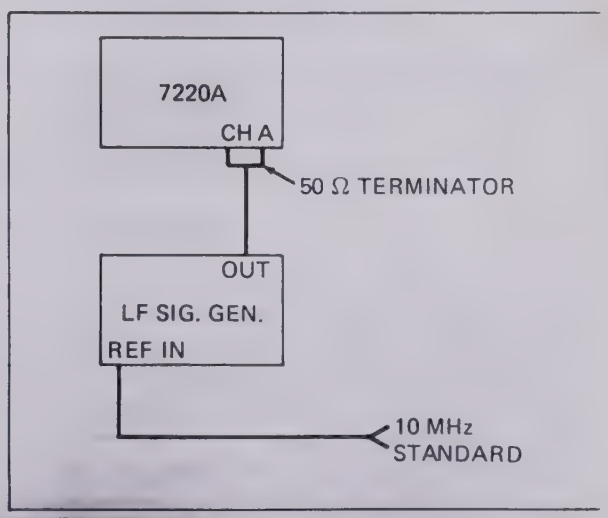


Figure 4-12. Standard Time Base Calibration

NOTE

The Low Frequency Signal Generator must be synchronized to a Standard Frequency Source for this procedure.

3. Set the Low Frequency Signal Generator to 10 MHz at 100 mV rms and connect it to the Channel A input with a 50 ohm terminator.

4. Using a non-ferrous adjustment tool, adjust the oscillator trimcap to obtain a display of 10.000000 MHz ± 57 Hz. 57 Hz is the maximum allowable deviation for this time base at this input frequency and resolution setting. The maximum allowable deviation can be found by multiplying the input frequency by the total accuracy, and adding the 1 count error (see Table 4-3). The oscillator trimcap is accessible through a hole at the left rear corner of the bottom of the 7220A (see Figure 4-13), so the 7220A will have to be turned on its side or top to perform this adjustment. If the tilt bail is mounted in the rear, it will have to be removed.

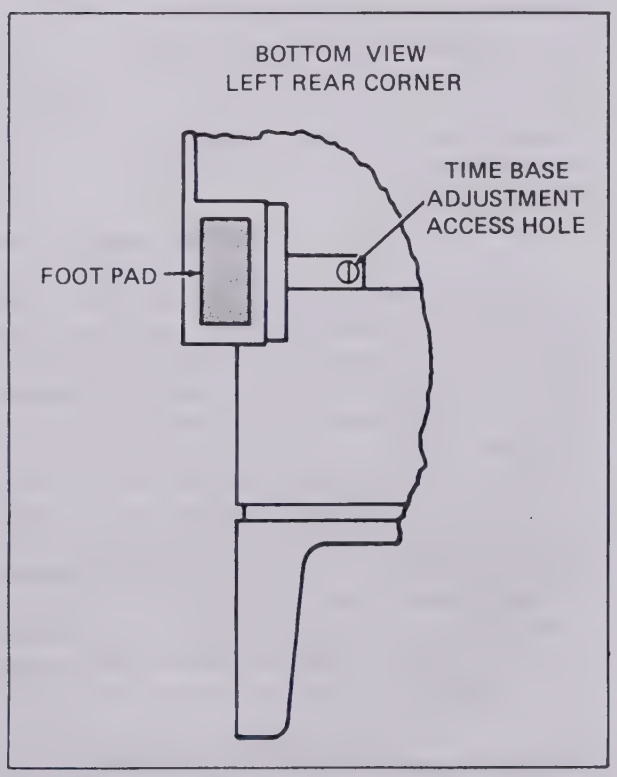


Figure 4-13. Time Base Adjustment Location

5. If adjustment does not yield the desired display, disconnect the 7220A line power cord, remove the top cover, and look at the top of the time base PCB (left rear corner of the Main PCB). Some of the Standard Time Bases are equipped with another trimcap on the top of the PCB for coarse adjustments. If your instrument has such a trimcap, refer to the Coarse Time Base Adjustment section which follows this section.

6. If the time base cannot be adjusted within the Specifications given in Section 1 and coarse adjustment is not available, refer to Troubleshooting.

7. After 24 hours, recheck any adjustment performed to verify stability.

4-46. Coarse Time Base Adjustment

4-47. Some of the Standard Time Bases have a coarse adjustment trimcap on the top of the PCB in addition to the fine adjustment trimcap which is accessible through a hole in the bottom of the instrument case (see Figure 4-13).

NOTE

Do not perform the Coarse Time Base Adjustment unless the Standard Time Base Calibration fails to bring the instrument within the specifications.

If it is determined that coarse adjustment is necessary, use the following procedure:

1. Set the fine time base adjustment to midrange.

2. Remove the 7220A top cover.

3. Follow steps 1, 2 and 3 of the Standard Time Base Calibration.

4. Using a non-ferrous adjustment tool, adjust the coarse adjustment trimcap to obtain a display as close as possible to 10.000000 MHz.

5. Install the 7220A top cover. Now perform the Standard Time Base Calibration.

4-48. TROUBLESHOOTING

4-49. Introduction

4-50. The material in the remainder of this section is presented as a troubleshooting aid for technicians. If the instrument fails to perform as expected, select the CHK function. If the instrument display is incorrect, the fault is in the instrument; if the display is correct, the fault may not lie in the instrument. Check the control settings for the 7220A. Also check the control settings, function, and interconnections of all associated equipment.

4-51. Sections 2 and 3 of this manual should be read and thoroughly understood before attempting to troubleshoot. As an aid to the troubleshooter, three additional subsections follow: Visual Inspection, Troubleshooting Guide, and Troubleshooting Techniques.

4-52. Whenever working with the instrument, follow procedures outlined on the yellow Static Awareness sheet located in this manual to prevent static discharge damage to CMOS and PMOS devices. Exercise special care when soldering to avoid damage to the instrument.

4-53. The instrument uses three basic types of logic: ECL, TTL, and CMOS. The circuits handling high frequency signals employ Emitter-Coupled Logic (ECL). Circuitry using CMOS ICs operate at CMOS logic levels. The remainder of the instrument employs Transistor-Transistor Logic (TTL). Table 4-8 lists typical high and low logic levels for each logic type.

Table 4-8. Typical Logic Levels

LOGIC TYPE	LOGIC 1	LOGIC 0
TTL	>2.4V	<0.6V
ECL	>4.1V	<3.2V
CMOS	>3.5V (>70% of supply)	<1.5V (<30% of supply)

4-54. Visual Inspection

4-55. Visual inspection can sometimes quickly locate instrument faults, saving the technician time. Use the Disassembly procedure presented earlier in this section to remove the top case cover. Carefully inspect the instrument, inside and out. Check for loose or broken wires and component leads, improperly seated plug-in assemblies, physically damaged components, discoloration due to arcing, or other obvious faults. Shorted capacitors or resistors in short paths are often discolored or burnt. Abusively high overloads may physically destroy carbon composition resistors, glass diodes, ceramic capacitors, thermistors, and other components. These symptoms or anything that looks suspect should be carefully checked before proceeding with involved troubleshooting.

4-56. Troubleshooting Guide

4-57. The Troubleshooting Guide, Table 4-9, provides some basic guidelines for locating the cause of improper operation. There are three basic cases of improper operation:

1. The instrument will not turn on. Check the main power supply per Table 4-9.

2. The instrument turns on, but the problems seem to be spread throughout the instrument or are erratic. This situation may be due to any of a number of power supply related problems. Check the power supplies per Table 4-9.

3. The instrument has a problem in one or more functions or ranges. Follow the guidelines in Table 4-9 for the appropriate circuit.

NOTE

See Figure 4-8 for the location of testpoints and identification of components. Use a 10X probe on the oscilloscope.

WARNING

TO AVOID SHOCK HAZARD, DO NOT TOUCH POWER SUPPLY COMPONENTS. LINE POWER VOLTAGE IS PRESENT FROM THE POWER CORD THROUGHOUT THE PRIMARY CIRCUIT OR THE MAIN POWER TRANSFORMER.

4-58. Troubleshooting Techniques

4-59. The following are techniques useful in isolating a fault in the instrument.

4-60. CURRENT TRACING

4-61. Current Tracer probes, such as the HP 547A, are usually the best way to locate shorts in the instrument. If the short is so bad that the power supply is loaded down, the Performance Checks may not provide any help in isolating the faulty circuit. Starting at the output of the loaded power supply, logically move the Current Tracer through the instrument until the short is found. The Current Tracer will glow brightest at the terminal of the shorted components. Shorted logic elements can be more difficult to locate because currents involved can be small.

4-62. HEATING AND COOLING

4-63. Alternately warming (with a heat gun) and cooling (with freon spray) of possible faulty circuits can provide a fast and effective troubleshooting technique for finding components that work intermittently.

4-64. MEASURING TEMPERATURE

4-65. Shorted components overheat. Resulting temperature differences can be monitored with the Fluke 80T-150 and any of its associated digital multimeters, or with the 8024 DMM with an accessory thermocouple attached.

Table 4-9. Troubleshooting Guide

PROBLEM	INSTRUCTIONS OR COMMENTS
Power Supply	Check ac power receptacle pins, power supplies, line voltage selector switches, Fuse F1. Check TP1, TP2, and TP3 for values listed in Table 4-7. Hint: If supplies are OK with front panel ON/STBY switch in STBY, but fail in ON, components outside the supplies may be shorted. Hint: Make certain that regulator ICs (U40, U41, and U42) are properly tightened to the heatsink, and that the heatsink is tightened to the circuit board.
Time Base and Clocking Signals	Be sure the rear panel REF switch is set to INT. Check: — You should see: TP4 — 10 MHz, TTL (clock) U19-13 — 1 MHz, TTL U19-3 — 100 kHz, TTL U28-7 — Approx. 63 kHz, CMOS (used only in Channel B) U28-3 — Approx. 61 Hz, CMOS (Scan rate clock that advances Sequencer U32) U15-40 — Approx. 1.2 kHz (U15 display oscillator)
Self Check, Control Logic and Counters	Set the CH A/CH B switch to CHK and set RESOLUTION to 10 Hz. Be sure the rear panel REF switch is set to INT. Display should be 10.00000 MHz. Refer to the Timing Diagram in Figure 3-7. Check: — You should see:
Sequencer	U32-4 (Q2 state) — Positive pulses, slightly wider than gate time of 0.1 sec. U32-3 (Q0 state) — Positive pulses U32-10 (Q4 state) — Positive pulses U32-1 (Q5 state) — Positive pulses U32-11 (Q9 state) — Positive pulses
Main Gate FF	U13-5 — Positive pulse, 0.1 sec. wide
Gate Synchronizer	U7-8 — Negative pulse, 0.1 sec. wide
Input Counters	U1-4 — 10 MHz, ECL U5-3 — 5 MHz, TTL when gate is on U6-9 — 1 MHz, TTL when gate is on U14-8 — 0.1 MHz, TTL when gate is on
Channel B	Set the front panel CH A/CH B switch to 1300 MHz. Check the Channel B power supplies: Input Fuse F2 TP8 — +5V TP9 — -1.8V U4-1 — +12V U4-23 — -12V

Table 4-9. Troubleshooting Guide (cont)

PROBLEM	INSTRUCTIONS OR COMMENTS
Channel B (cont)	Apply a signal to Channel B input within specifications (100-1300 MHz, 40 mV-5V rms)
	Q6 collector — TTL low U3-4 — Input/4, ECL U3-2 — Input/16, ECL U1-4 — Input/16, ECL
Channel B BURST	Set the front panel CH A/CH B switch to 1300 BURST. Apply signal to Channel B as above, only in bursts at least as long as 40 ms + gate time (see Table 3-1 for gate times).
	U21-6 — Low, CMOS U21-3 — Positive pulses, CMOS, same width as input bursts U21-2 — Pulses U1-4 — Input/16, ECL
Channel A (front panel)	Hint: If excessive input voltages have been applied to the Channel A input, it is likely that Q1 is damaged, or that CR1 or CR2 are leaky.
	Set front panel CH A/CH B switch to 125 MHz. Apply signal to Channel A input between 10 Hz and 125 MHz, and at a level equal to the sensitivity specification at the frequency used. Set attenuation controls to X1 and fully CCW. If necessary, refer to the Disassembly instructions and remove the front panel first.
	Q1-Drain — Approx. +11.5V Q1-Gate — Same as input U1-11 — Same as input U1-12 — -5V U1-2 and U1-3 — Approx. square wave, same frequency as input, ECL U1-18 — Approx. square wave, same frequency as input, TTL
Display	Hint: To test the LEDs, press and hold front panel RESET to turn on all segments. If only one segment is dark, suspect the LED. If an entire digit is dark, or the same segment on all digits is dark, suspect the digit drive or segment drive electronics respectively.
	To test decimal points, remove any inputs to the 7220A. Set POWER to ON. Set the CH A/CH B switch to RES MULT and check for a single decimal point at each RESOLUTION setting. Set the CH A/CH B switch to any other setting and check for a single decimal point at each RESOLUTION setting.
	Also check:
	U15-40 — Approx. 1.2 kHz pulses (display clock) U15-2 — Positive pulses, 22% duty factor (digit strobes 8 and 9) U15 pins 3 through 9 — Positive pulses, 11% duty factor (digit strobes 7 through 1) U18-4 — Positive pulse, 11% duty factor (digit strobe 9)
	Set CH A/CH B switch to CHK and RESOLUTION to 100 Hz with no signal inputs.
	U35-2 — Positive pulse, 66% duty factor (leading zeros blanking)

TRANSMISSION REPORT

11.06.1998 14:09

GTE ERS METROLOGY (972) 487-2083

DATE TIME	DURATION	REMOTE ID	MODE	PAGES	RESULT
11.06 13:58	10'53"	12194286124	ECM	17	O.K.

Section 5
List of Replaceable Parts

TABLE OF CONTENTS

ASSEMBLY NAME	DRAWING NO.	TABLE NO.	TABLE PAGE	FIGURE NO.	FIGURE PAGE
7220A Final Assembly	7220A-T&B, 5001	5-1	5-4	5-1	5-5
A1 Main PCB Assembly	7220A-4001T	5-2	5-8	5-2	5-10
A2 Front Panel PCB Assembly	7220A-4002T	5-3	5-11	5-3	5-12
A3 Timebase PCB Assembly	7220A-4009	5-4	5-13	5-4	5-13

5-1. INTRODUCTION

5-2. This section contains an illustrated list of replaceable parts for the instrument. A similar parts listing for each option will be found in Section 6. Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed first by reference designation. Each assembly is accompanied by an illustration showing the location of each part and its reference designator.

5-3. The parts lists contain the following information:

- Reference Designator
- Description
- Fluke Stock Number
- Federal Supply Code for Manufacturers (see end of this section for code-to-name list).
- Manufacturer's Part Number
- Total Quantity of Components per Assembly

5-4. HOW TO OBTAIN PARTS

5-5. Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. and its authorized representatives by using the part number under the heading FLUKE STOCK NO. A list of federal supply codes is provided at the end of this section. In the event that a part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

5-6. To ensure prompt and efficient handling of your order, please include the following information:

- Quantity
- Fluke Stock Number
- Description
- Reference Designation
- Printed Circuit Board Part Number and Revision
- Instrument Model Number and Serial Number

5-7. Parts price information is available from the John Fluke Manufacturing Co., Inc or its representative. Prices are also found in the Fluke Replacement Parts Catalog, with is available on request.

5-8. MANUAL STATUS INFORMATION

5-9. The following Manual Status Information table defines assembly revision levels documented in this manual. To identify the configuration of the pcb's used in your instrument, refer to the revision letter (marked in ink) on the component side of the pcb.

5-10. TECHNICAL SERVICE CENTERS

5-11. A list of technical service centers is included at the end of this section.

Manual Status Information

REF OR OPTION NO.	ASSEMBLY NAME	FLUKE PART NO.	X = The PCA revision levels documented in this manual.																									
			–	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
A1	Main PCB	471540																								X			
A2	Front Panel PCB	471516																					X						
A3	Timebase PCB	538660	X																										
-010	Battery Option	475962													X														
-351	Resolution Multiplier Option	481747	X																										
-521	Digital Interface Option	487454					X																						

Table 5-1. 7220A Final Assembly
(See Figure 5-1.)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY	NOT
A 1		MAIN PCB ASSEMBLY	471540	89536	471540	1	
A 2		FRONT PANEL ASSEMBLY	471516	89536	471516	1	
A 3		TIMEBASE PCB ASSEMBLY	476572	89536	476572	1	
F 1		FUSE,.25X1.25,0.25A,250V,SLOW	166306	71400	MDL1-4	1	
H 1		SCREW,MACH,FH,P,STL,6-32X0.625	114876	COMMERCIAL		6	
H 2		SCREW,THD FORM,PHP,STL,6-20X3/8	288266	COMMERCIAL		1	
H 3		SCREW,THD FORM,PH,P,STL,6-32,.375	485227	COMMERCIAL		6	
H 4		WASHER,LOCK,EXTRNL,STEEL,0.500 ID	175943	COMMERCIAL		1	
H 5		WASHER,SHLDR,NYLON,.113,.245	485417	COMMERCIAL		2	
H 6		SCREW,MACH,PH,P,STL,4-40X0.625	145813	COMMERCIAL		2	
H 7		WASHER,LOCK,INTRNL,STEEL,#4	110403	COMMERCIAL		2	
H 8		NUT,MACH,HEX,STL,4-40	110635	COMMERCIAL		2	
H 9		SCREW,MACH,PH,P,SEMS,STL,6-32X.500	177030	COMMERCIAL		2	
H 10		NUT,CAP EXT LW,STL,6-32X.109	152819	COMMERCIAL		4	
H 11		NUT,HEX,STL/BR,15/32-32	110916	COMMERCIAL		1	
H 12		SCREW,MACH,PH,P,STL,4-40X0.500	152132	COMMERCIAL		2	
H 13		WASHER,LOCK,SPLIT,STEEL,#4	110395	COMMERCIAL		2	
MP 1		LATCH	467548	89536	467548	2	
MP 2		TOP COVER ASSY	509414	89536	509414	1	
MP 3		SPEC DECAL	483032	89536	483032	1	
MP 4		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1	
MP 5		CONNECTOR COVER	488395	89536	488395	1	
MP 6		REAR PANEL	475939	89536	475939	1	
MP 7		HEAT SINK	473868	89536	473868	1	
MP 8		CONN,COAX,BNC(F),PANEL	152033	52500	30355-1	2	
MP 9		HLDR PART,FUSE,CAP,1/4X1-1/4	460238	61935	031.1666	1	
MP 10		INSULATED BUSHING	488429	89536	488429	2	
MP 11		TERM,RING,3/8 & 7/64,SOLDR	441972	79963	761	1	
MP 12		INSUL PART,TRANS,SILICONE,POWER	534453	55285	7403-09FR-54	2	
MP 13		LABEL,WARNING	386250	89536	386250	1	
MP 14		BOTTOM COVER ASSY	489302	89536	489302	1	
MP 15		BUTTON GREEN	486498	89536	486498	1	
MP 16		BUTTON LIGHT PUTTY GRAY	486480	89536	486480	1	
MP 17		BUTTON BLUE	486472	89536	486472	1	
MP 18		GROMMET,MOLDED,RUBBER,.187,.312	104273	2K262	215-006	1	
MP 19		INSULATOR,TRANSFORMER	507517	89536	507517	1	
MP 20		FLEX STRIP	605212	89536	605212	3	
MP 21		FRONT PANEL	478396	89536	478396	1	
MP 22		KNOB ASSY 1/8IN SHAFT MED P.G.	490755	89536	490755	1	
MP 23		OSCILLATOR,10MHZ,OVENED,5V TESTED	516096	89536	516096	1	
MP 24		INSULATOR OSCILLATOR	487710	89536	487710	1	
T 1		TRANSFORMER	486514	89536	486514	1	
TM 1		INSTRUCTION MANUAL	487488	89536	487488	1	
U 39	*	IC,VOLT REG,FIXED,-5 VOLTS,1.5 AMPS	394551	04713	MC7905CT	1	
U 40	*	IC,VOLT REG,FIXED,+12 VOLTS,1.5 AMPS	413195	04713	MC7812CT	1	
U 41	*	IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	12040	LM317T	1	
W 1		CORD,LINE,5-15/IEC,3-18AWG,SVT	343723	70903	17237	1	
W 2		AC CABLE 1	504068	89536	504068	1	
W 3		AC CABLE 2	504050	89536	504050	1	
W 4		AC CABLE 3	504076	89536	504076	1	
W 5		7220A CHAN B COAX CABLE ASSY	539833	89536	539833	1	
XF 1		HLDR PART,FUSE,BODY 1/4X1-1/4,5X20MM	460329	61935	031.1673	1	

An * in 'S' column indicates a static-sensitive part.

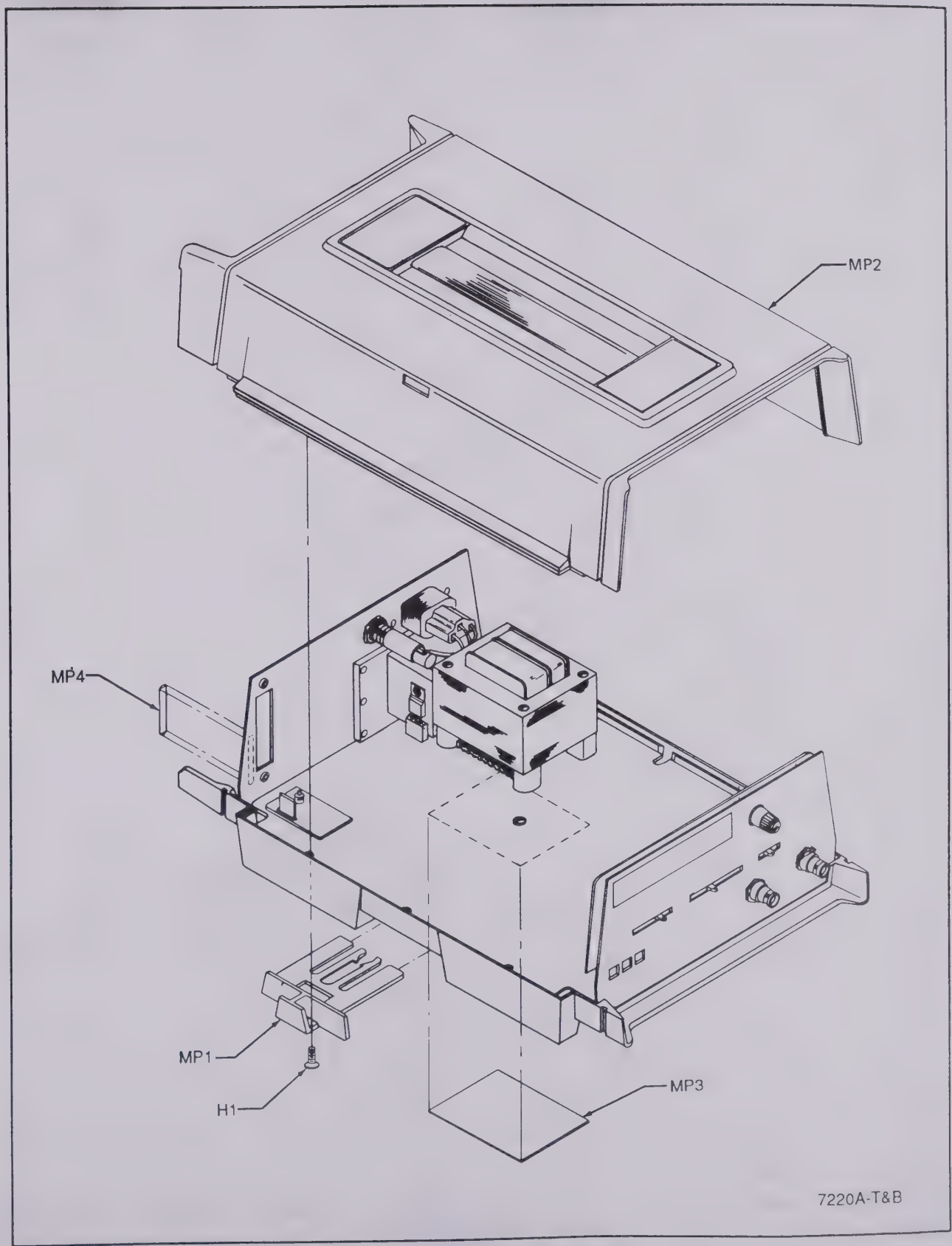


Figure 5-1. 7220A Final Assembly

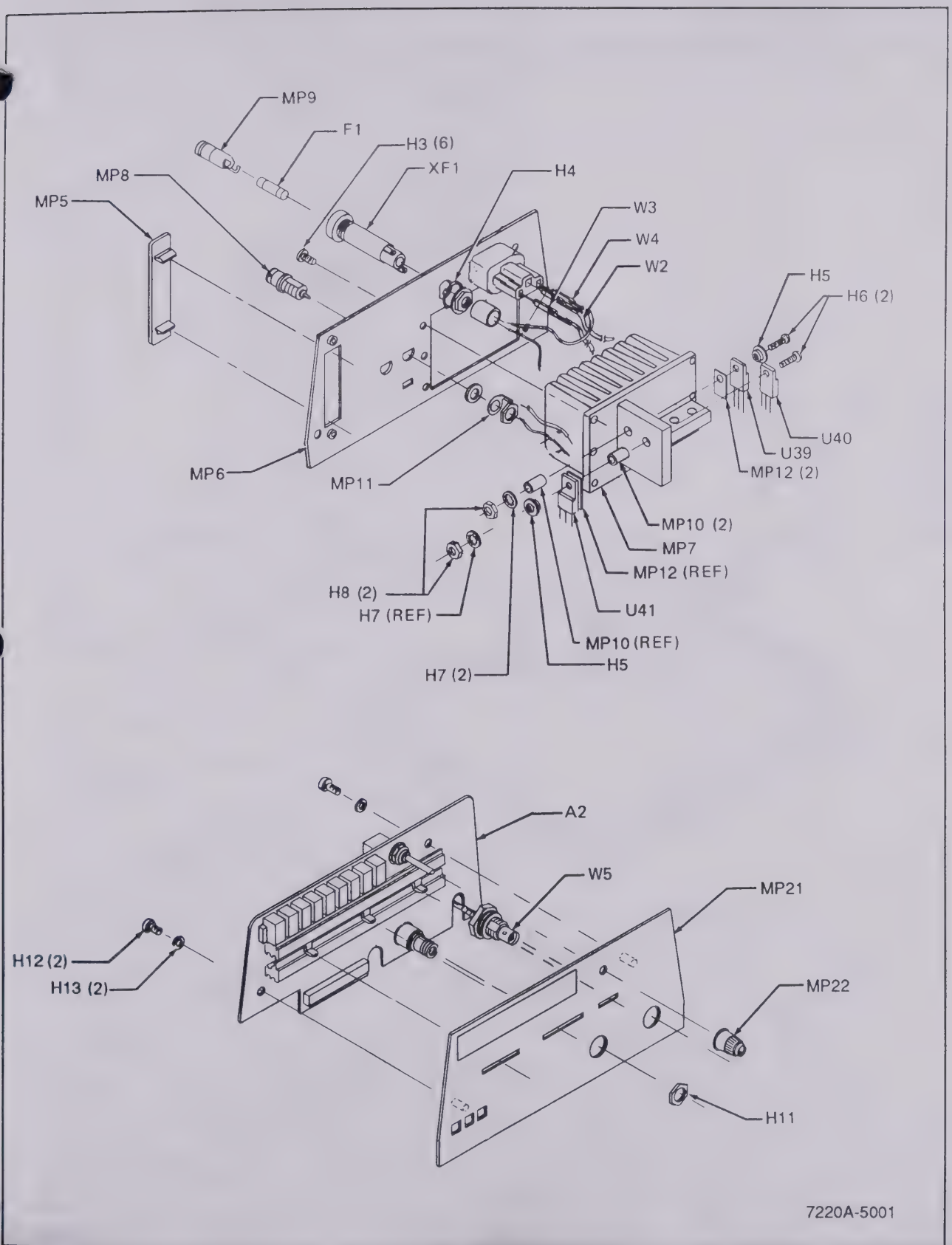


Figure 5-1. 7220A Final Assembly (cont)

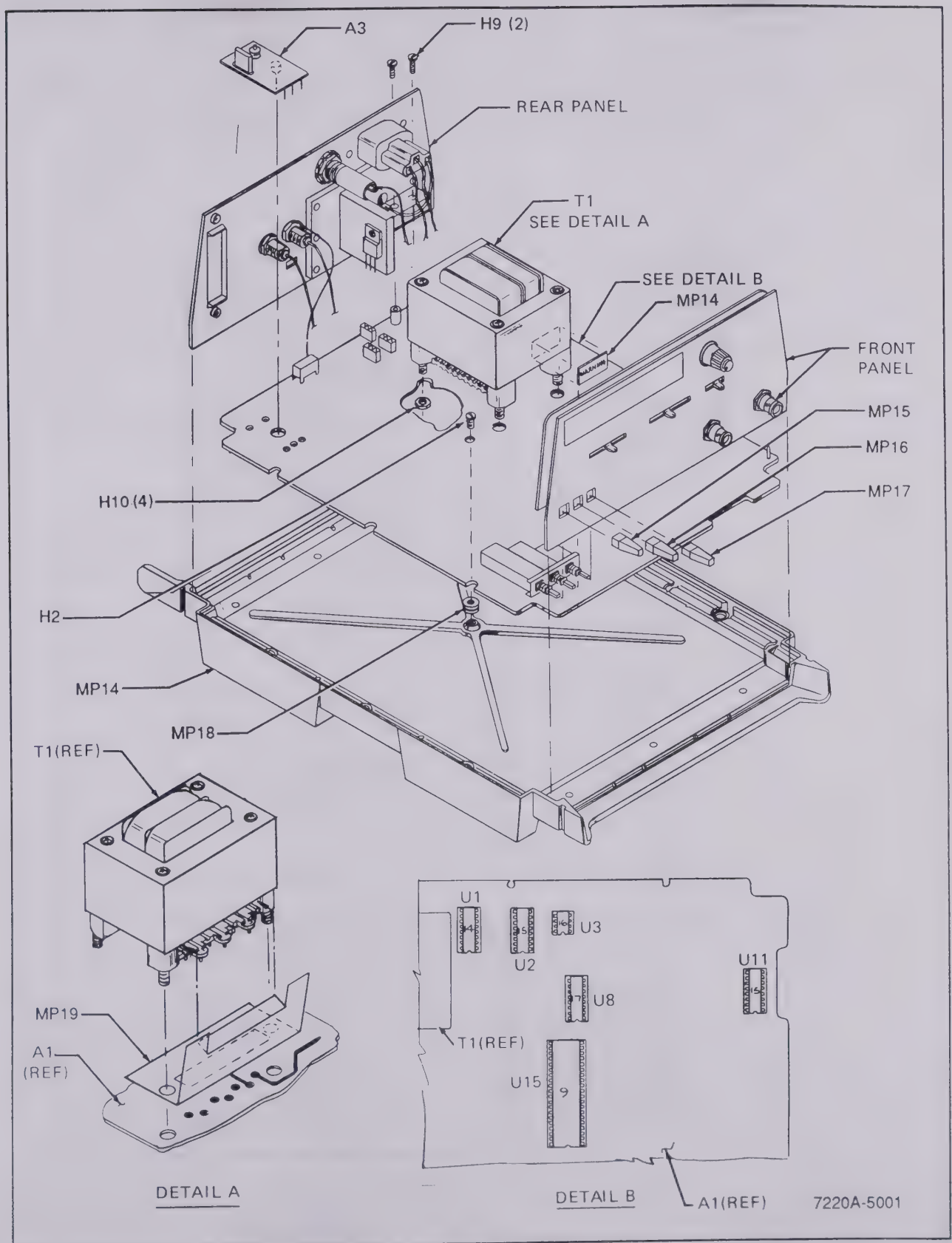


Figure 5-1. 7220A Final Assembly (cont)

Table 5-2. A1 Main PCB Assembly
(See Figure 5-2.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
C 1- 3		CAP,AL,470UF,+50-20%,50V	478792	62643	SM16 VB-471	3	
C 4		CAP,AL,4700UF,+30-10%,16V,SOLV PROOF	460261	62643	KME16VN472K23X27LLV	1	
C 5- 7, 10,		CAP,TA,10UF,+-20%,20V	330662	56289	199D106X0020CA2	32	
C 11, 14, 17,			330662				
C 18, 21- 23,			330662				
C 29, 32- 50,			330662				
C 52			330662				
C 8, 9, 24,		CAP,CER,0.01UF,+80-20%,100V,Z5V	149153	60705	562CZ5UCK101AF103Z	5	
C 26, 27			149153				
C 13		CAP,TA,22UF,+-20%,15V	423012	56289	199D226X0015DA2	1	
C 15, 16, 19,		CAP,CER,0.01UF,+-20%,100V,X7R	407361	04222	3419-1000-103M	5	
C 20, 51			407361				
C 25		CAP,CER,0.1UF,+-20%,100V,Z5V	149146	60705	565CZ5UBA101AW104M	1	
C 30		CAP,POLYES,0.0022UF,+-10%,50V	313239	80031	713D1BH222K500SK	1	
C 31		CAP,TA,330UF,+-10%,6V	193011	31433	T310D337K006AS	1	
CR 1, 2		DIODE,SI,RECT,BRIDGE,BV=200V,IO=1.0A	296509	30800	KBP 02M	2	
CR 3, 4		DIODE,SI,50 PIV,2.0 AMP	347559	14936	P-300A-031	2	
CR 6	*	DIODE,SI,BV=75V,IO=150MA,500MW	203323	07910	1N4448	1	
CR 7, 8	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	2	
F 2, 3		FUSE,.25X.35,0.2A,125V,FAST,RADIAL	370577	75915	273.2000	2	
J 1		CONN,COAX,SMB(M),PWB	352450	98291	51-051-0000-220	1	
J 2- 24		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	23	
JB 1, 2		PIN,SINGLE,PWB,0.025 SQ	379438	00779	1-87022-0	15	
L 1, 2		CHOKE,6TURN	320911	89536	320911	2	
MP 1		SPACER,SWAGED,RND,BR,4-40,.437	442913	9W423	9534B-B-0440	1	
MP 2		SPACER,SWAGED,RND,BR,6-32,.250	446351	9W423	9533B-B-0440	2	
Q 1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	04713	2N3906	1	
Q 2	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	352369	12040	2N4403	1	
Q 3, 4, 6,	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	4	
Q 9	*		218396				
Q 5	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	330803	04713	MPS6560	1	
Q 7, 8	*	TRANSISTOR,SI,PNP,HI-SPEED SWITCH	369629	04713	2N5771	2	
R 1		RES,CF,1.8K,+-5%,0.25W	573220	59124	CF1-4182JB	1	
R 2		RES,CF,180,+-5%,0.25W	573048	59124	CF1-4 181 J B	1	
R 3, 21, 26		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4101JB	3	
R 4, 6		RES,CF,470,+-5%,0.25W	343434	80031	1-4-5P470E	2	
R 5, 29, 42,		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4472JB	5	
R 48, 59			573311				
R 7, 52		RES,CF,150,+-5%,0.25W	573030	59124	CF1-4151JB	2	
R 8, 66		RES,CF,27,+-5%,0.25W	641357	59124	CF1-4 270 J B	2	
R 9		RES,CF,47K,+-5%,0.25W	573527	59124	CF1-4 473 J B	1	
R 10		RES,CF,2.4K,+-5%,0.25W	573253	57668	R25J2K4	1	
R 11, 53, 55,		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4103JB	4	
R 56			573394				
R 12		RES,MF,301,+-1%,0.125W,100PPM	267740	91637	CMF-55 3010 F T-1	1	
R 13		RES,MF,43.2,+-1%,0.125W,100PPM	296731	01121	MFF1-843R2F	1	
R 14		RES,VAR,CERM,50,+-10%,0.5W	447862	80294	3386R-1-500	1	
R 19, 24		RES,CF,100,+-5%,0.25W	348771	59124	CF1-4 101 J	2	
R 22, 23, 54,		RES,CF,10K,+-5%,0.25W	348839	59124	CF1-4 102 J B	5	
R 62, 63			348839				
R 25, 35, 36		RES,CF,4.7K,+-5%,0.25W	348821	59124	CF1-4 472 J B	3	
R 27, 30, 31		RES,CF,560,+-5%,0.25W	385948	80031	5043C225560R0J	3	
R 28, 40, 41,		RES,CF,560,+-5%,0.25W	573147	59124	CF1-4561JB	6	
R 43, 50, 51			573147				
R 32		RES,CF,150,+-5%,0.25W	343442	59124	CF1-4 151 J B	1	
R 33		RES,CF,330K,+-5%,0.25W	376640	80031	1-4-5P330K	1	
R 34		RES,CF,1M,+-5%,0.25W	348987	80031	1-4-5P1M	1	
R 37, 39, 57,		RES,CF,1K,+-5%,0.25W	343426	59124	CF1-4 102 J B	4	
R 60			343426				
R 38		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4102JB	1	
R 44		RES,CF,390,+-5%,0.25W	573105	59124	CF1-4 391 J B	1	
R 45		RES,CF,390,+-5%,0.25W	441543	80031	1-4-5P390E	1	
R 46, 47		RES,CF,240,+-5%,0.25W	573063	59124	CF1-4 240 J B	2	
R 49		RES,CF,27,+-5%,0.25W	348763	59124	CF1-4 27R0 J	1	
R 58		RES,CF,6.8K,+-5%,0.25W	368761	80031	1-4-5P6K8	1	
R 61		RES,CF,5.1K,+-5%,0.25W	573329	59124	CF1-4512JB	1	
R 64		RES,CF,1.3,+-5%,0.25W	572891	59124	CF1-4 1R3 JB	1	
R 65, 67		RES,CF,330,+-5%,0.25W	573089	59124	CF1-4 331 J B	2	
R 68		RES,MF,1K,+-1%,0.125W,100PPM	168229	91637	CMF551001F T-1	1	

An * in 'S' column indicates a static-sensitive part.

Table 5-2. A1 Main PCB Assembly (cont)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R 69		RES,VAR,CERM,200,+-10%,0.5W	275743	32997	3386R-1-201	1	
R 70		RES,MF,3.01K,+-1%,0.125W,100PPM	312645	91637	CMF553011F T-1	1	
R 71		RES,CF,330,+-5%,0.25W	368720	80031	1-4-5P330E	1	
S 1- 3		PUSH BUTTON ASSEMBLY	473991	89536	473991	1	
S 4, 5		SWITCH,SLIDE,DPDT,POWER	234278	82389	11A1297A	2	
S 8		SWITCH,SLIDE,DPDT	354878	95146	MSS-2250R	1	
U 1	*	IC,ECL,JK M/S F/F,+EDG TRG,W/SET&CLR	402743	07263	F95029DC	1	
U 2, 11	*	IC,ECL,TRIPLE LINE RECEIVER	369702	04713	MC10116P	2	
U 3	*	IC,ECL,1GHZ DIV BY 4 PRESCALER	472787	04713	SC62954L	1	
U 4		1300MHZ AMP/DIV TESTED	490664	89536	490664	1	
U 5	*	IC,STTL,QUAD 2 INPUT AND GATES	477539	01295	SM74SON	1	
U 6, 13	*	IC,STTL,DUAL JK F/F,+EDG TRIG	363440	01295	SN74S112N	2	
U 7	*	IC,STTL,DUAL D F/F,+EDG TRG,W/SET&CLR	418269	01295	SM74S74N	1	
U 8	*	IC,ECL,QUAD 2 INPUT NOR GATE	680819	04713	MC10102P	1	
U 9	*	IC,TTL,QUAD 2-1 LINE MUX W/STROBE	403576	01295	SN74157N	1	
U 10	*	IC,OP AMP,GENERAL PURPOSE,TO-5 CASE	284760	04713	308H	1	
U 12	*	IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	04713	SN74LS02N	1	
U 14, 23	*	IC,TTL,DIV BY 2,DIV BY 5 COUNTER	293159	01295	SN7490AN	2	
U 15	*	IC,MOS,6DEC UP CNTR W/8DEC LATCH&MUX	473215	55261	LS7031-F	1	
U 16	*	IC,TTL,QUAD D F/F,+EDG TRG,W/MSTR CLR	355057	18324	N74175N	1	
U 17	*	IC,CMOS,BCD-7SEG LTCH/DCDR/DRVR	429522	04713	MC14511BCP	1	
U 18, 22	*	IC,CMOS,HEX INVERTER	381848	02735	CD4049AE	2	
U 19	*	IC,LSTTL,DUAL DIV BY 2,DIV BY 5 CNTR	483594	01295	SN74LS390N	1	
U 20	*	IC,MOS,COUNTER TIME BASE CIRCUIT	381822	60496	5009N	1	
U 21, 34, 35	*	IC,CMOS,DUAL D F/F,+EDG TRIG	340117	04713	MC14013CL	3	
U 24	*	IC,CMOS,TRIPLE 3 INPUT OR GATE	408575	04713	MC14075BCP	1	
U 25, 36	*	IC,TTL,MOS-LED 6SEGMENT DRIVER	429506	27014	DS75492N	2	
U 26	*	IC,CMOS,QUAD AND-OR SELECT GATE	419010	54590	CD4019BE	1	
U 27	*	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	04713	SN74LS14N	1	
U 28	*	IC,CMOS,14STAGE RIPPLE CARRY BIN CNTR	394486	04713	MC14020BCP	1	
U 29	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	04713	SN74LS00N	1	
U 30	*	IC,CMOS,HEX BUFFER	381830	04713	MC14050BCP	1	
U 31	*	IC,CMOS,TRIPLE 3 INPUT NAND GATE	375147	04713	MC14023BCP	1	
U 32	*	IC,CMOS,DIV BY 10CNTR W/10DECODED OUT	403568	04713	MC14017BCP	1	
U 33	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	04713	MC14001BCP	1	
U 37, 38	*	IC,CMOS,QUAD BILATERAL SWITCH	363838	02735	CD4016AE	2	
U 42	*	IC,VOLT REG,FIXED,-12 VOLTS,0.1 AMPS	473819	04713	MC79L12ACP	1	
U 43	*	IC,BPLR,TIMER,8 PIN DIP	402610	18324	NE555N	1	
VR 5	*	ZENER,UNCOMP,5.6V,5%,20.0MA,0.4W	277236	04713	1N752A	1	
XF 2, 3		SOCKET,SINGLE,PWB,FOR 0.018-0.025 PIN	403642	00779	50863-8	4	
XU 1, 2, 8,		SOCKET,IC,16 PIN	276535	00779	2-640358-1	4	
XU 11			276535				
XU 3		SOCKET,IC,8 PIN	478016	00779	2-640463-1	1	
XU 15		SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
Z 1		RES,CERM,DIP,14 PIN,7 RES,39,+-5%	412866	91637	MDP14-03-390J	1	
Z 2		RES,CERM,SIP,8 PIN,7 RES,4.7K,+-2%	412916	80294	4608H-101-472	1	

An * in 'S' column indicates a static-sensitive part.

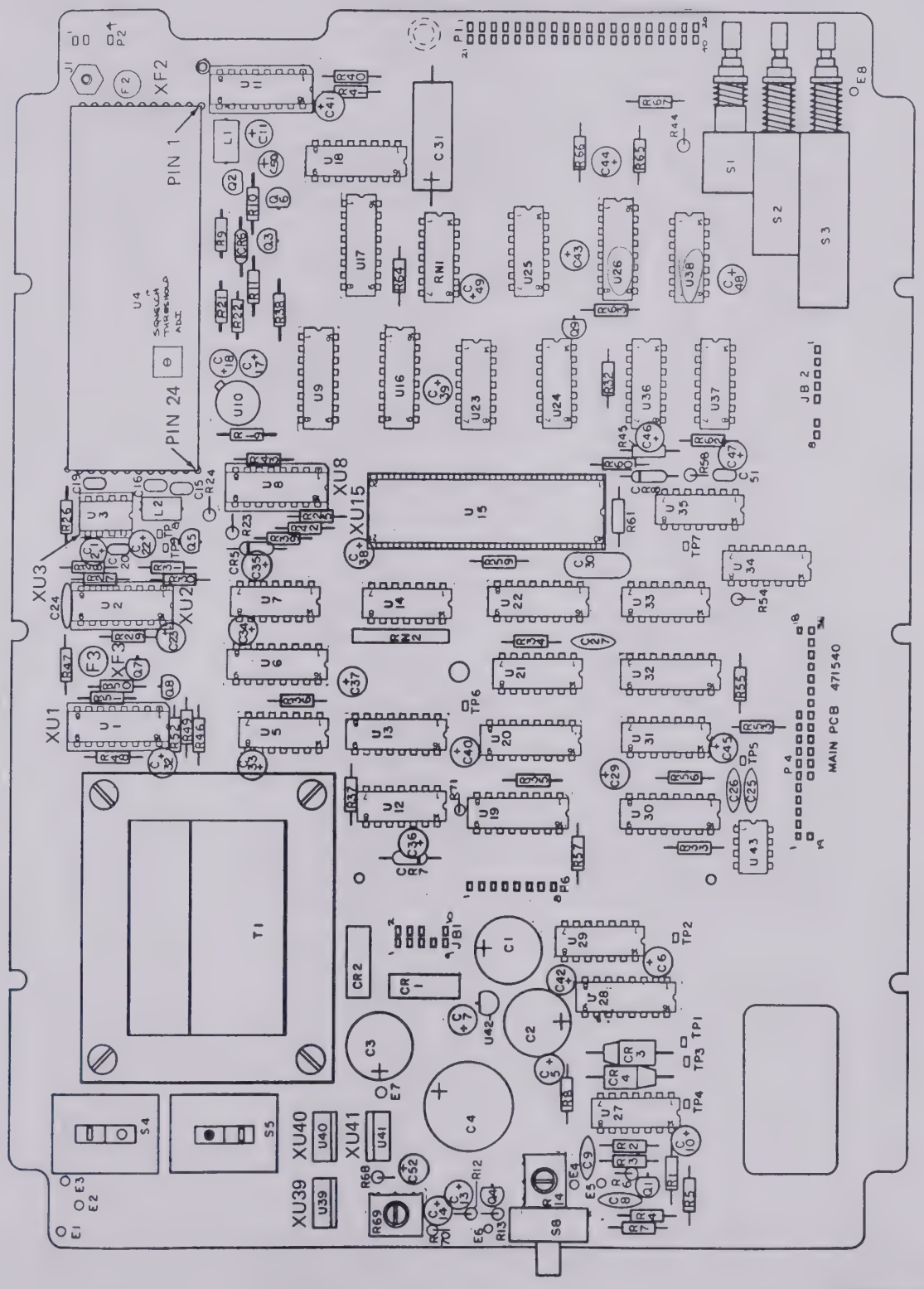


Figure 5-2. A1 Main PCB Assembly

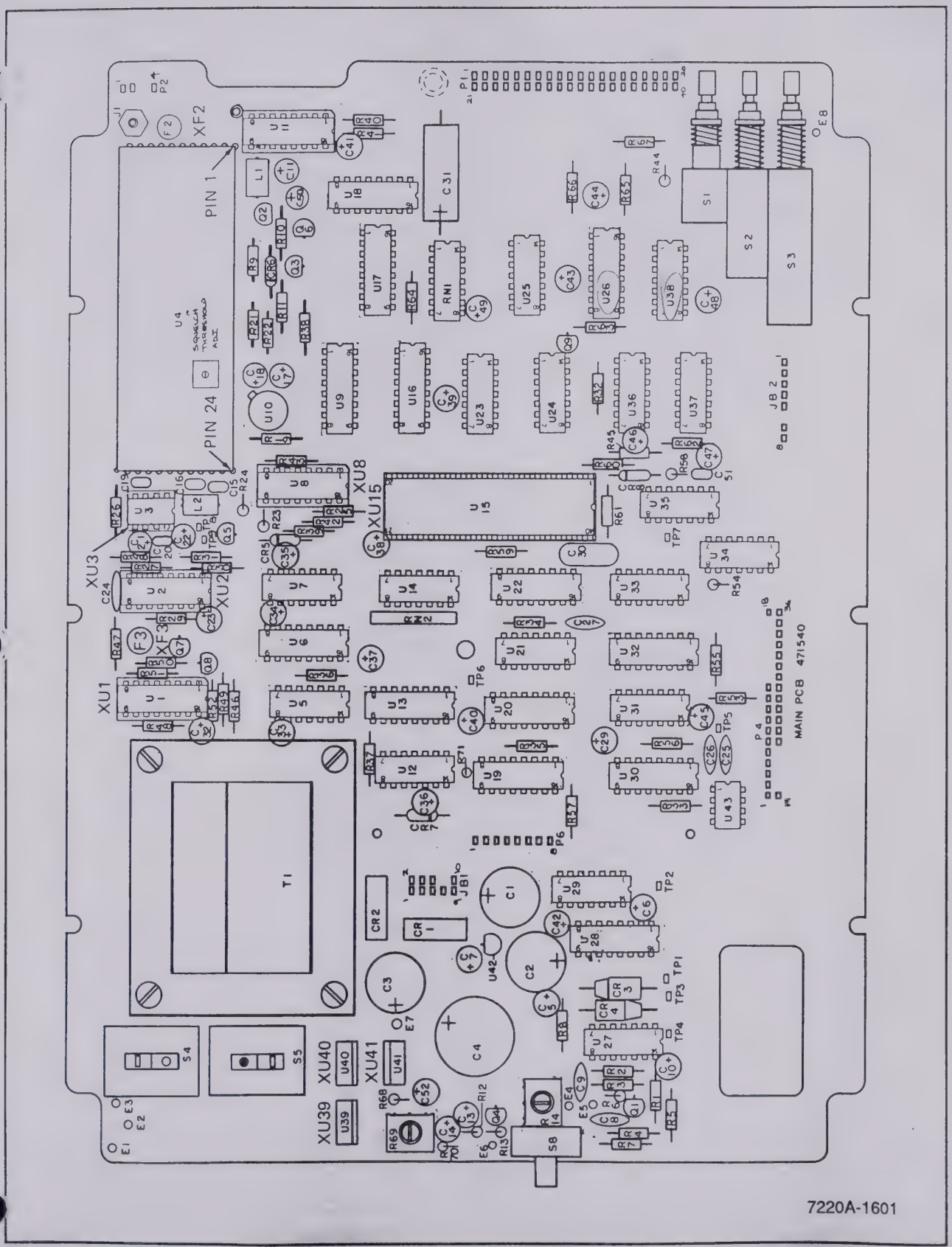


Figure 5-2. A1 Main PCB Assembly

Table 5-3. A2 Front Panel PCB Assembly
(See Figure 5-3.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
C 1		CAP,POLYES,0.068UF,+-20%,250V	478651	89536	478651	1	
C 2		CAP,CER,7.5PF,+-0.25PF,1000V,C0J	519082	59660	868-000-C0H0-759C	1	
C 3		CAP,CER,500PF,+-10%,1000V,X5R	105692	60705	562CX5FCK102EE501K	1	
C 4, 10, 17,		CAP,TA,10UF,+-20%,15V	193623	56289	195D106X0015A1	4	
C 18			193623				
C 5		CAP,CER,100PF,+-10%,100V,C0G	557322	51406	RPE110C0G101K1	1	
C 6		CAP,TA,22UF,+-20%,15V	519074	56289	199D226X1016DA1	1	
C 7, 11, 13,		CAP,CER,1000PF,+-20%,100V,X7R	816181	51406	RPE121911X7R102M100VPT	5	
C 15, 19			816181				
C 8, 9		CAP,TA,39UF,+-20%,6V	163915	56289	196D396X0006KA1	2	
C 12		CAP,MICA,390PF,+-5%,500V	148437	09023	CD15FD391J	1	
C 14		CAP,MICA,39PF,+-5%,500V	148544	09023	CD15ED390JO	1	
CR 1, 2	*	DIODE,SI,BV=30V,IO=150MA,250MW	707521	07263	FJT1100	2	
DS 1- 9		DIODE,LED,RED,7 SEGMENT,NUMERIC	742312	28480	HDSP-7303	9	
DS 10-12		LED,RED,ARRAY	483420	28480	HLMP6203	1	
H 1		SCREW,THD FORM,PH,P,STL,2-28,.406	493957	COMMERCIAL		8	
J 1		SOCKET,2 ROW,PWB,0.100C,RT ANG,40 POS	460030	00779	4-102084-6	1	
J 2- 4		SOCKET,SINGLE,PWB,FOR 0.025 PIN	375329	00779	85863-3	3	
L 1		CHOKE,6TURN	320911	89536	320911	1	
MP 1		SWITCH PART,ACTUATOR,PCB SLIDE	454371	00779	435371	3	
MP 2		SWITCH PART,DETENT SPRING,PCB SLIDE	472878	00779	435996	3	
MP 3		SWITCH PART,WIPER GUIDE,PCB SLIDE	472886	00779	435998	3	
MP 4		SWITCH PART,CARRIER,PCB SLIDE,16 POS.	477976	00779	435999-9	2	
MP 5		SOCKET,SINGLE,PWB,FOR 0.080 PIN	149112	74970	105-0753	1	
MP 6		CONN,COAX,BNC(F),PWB	479162	24931	28JR175	1	
Q 1	*	TRANSISTOR,SI,N-JFET,TO-92	288324	17856	J2067	1	
Q 2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	
R 1		RES,CC,910K,+-5%,0.25W	285338	01121	CB9145	1	
R 2		RES,CC,100K,+-5%,0.25W	148189	01121	CB1045	1	
R 3		RES,CC,220K,+-5%,0.5W	109025	01121	EB2245	1	
R 4		RES,CF,150,+-5%,0.25W	343442	59124	CF1-4 151 J B	1	
R 5		RES,CF,12K,+-5%,0.25W	348847	80031	1-4-5P12K	1	
R 6		RES,CF,2.7K,+-5%,0.25W	386490	80031	1-4-5P2K7	1	
R 7, 8		RES,MF,1.5K,+-1%,0.125W,100PPM	313098	91637	CMF-55 1501 F T-1	2	
R 9		RES,CF,470K,+-5%,0.25W	342634	80031	1-4-5P474K	1	
R 10		RES,VAR,CERM,25K,+-10%,0.5W	289678	80294	3386S-1-253	1	
R 11		RES,VAR,CERM,5K,+-20%,0.5W	226084	80294	3329H-1-502	1	
R 12		RES,VAR,CP,25K,+-30%,1W	485664	12697	CM46142	1	
R 13, 14		RES,CF,10K,+-5%,0.25W	348839	59124	CF1-4 102 J B	2	
R 15		RES,CF,180,+-5%,0.25W	441436	59124	CF1-4 181 J B	1	
R 17, 18		RES,CF,560,+-5%,0.25W	385948	80031	5043C225560R0J	2	
U 1	*	IC,BPLR,AMP W/SCHMT TRIG,DC TO 125MHZ	429191	32719	429191	1	
U 2	*	IC,VOLT REG,FIXED,-5.0 VOLTS,0.1 AMPS	454793	04713	MC79L05ACP	1	
XU 1		SOCKET,IC,18 PIN	418228	91506	218-AG39D	1	
Z 1		RES,CERM,SIP,8 PIN,7 RES,10K,+-2%	412924	91637	CSC08A-01-103G	1	
Z 2		RES,CERM,SIP,10 PIN,9 RES,10K,+-2%	414003	91637	CSC10A-01-103G	1	

An * in 'S' column indicates a static-sensitive part.

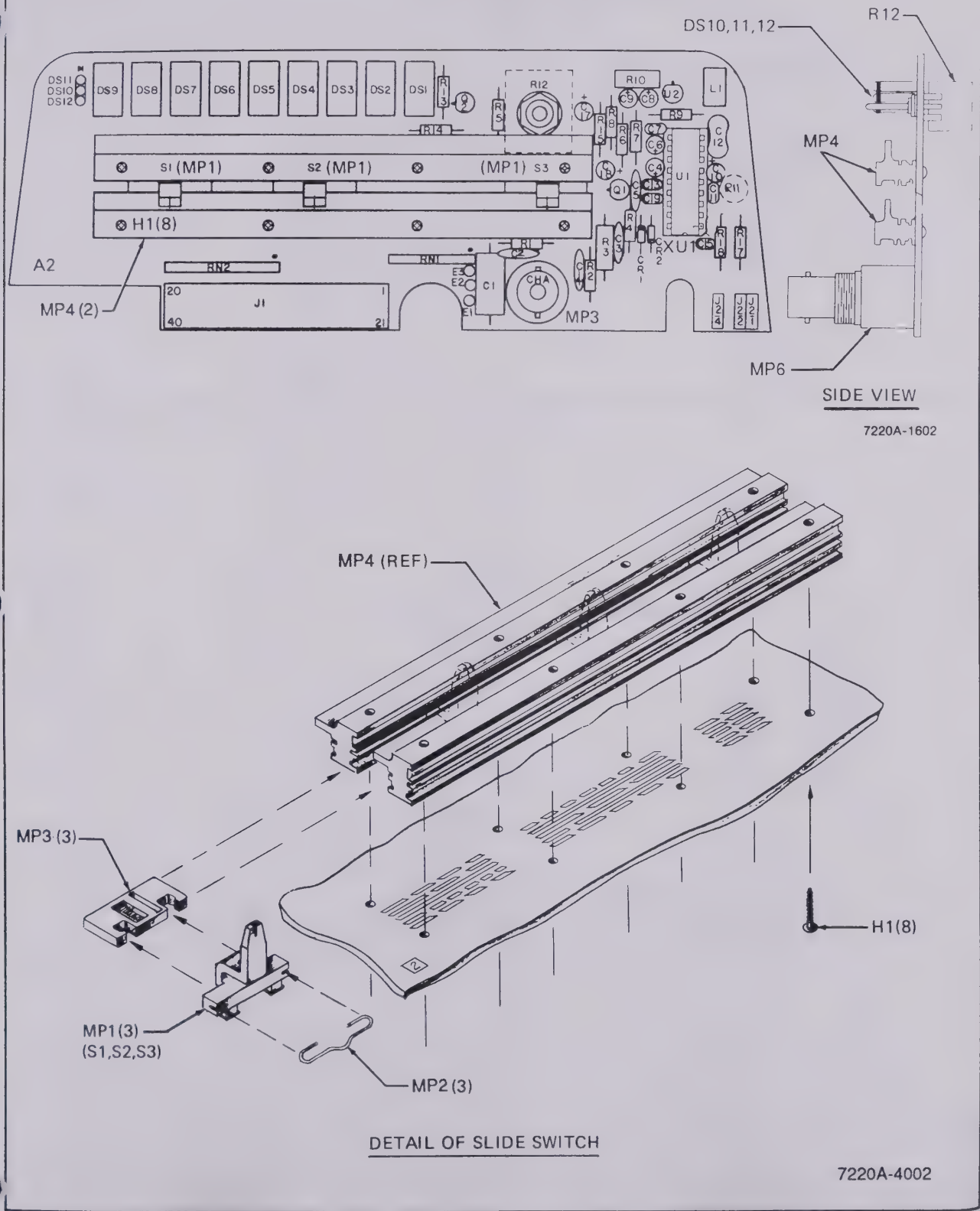
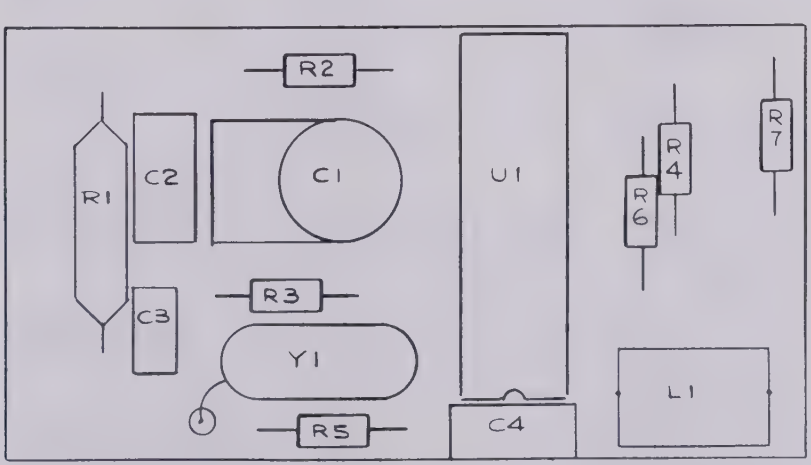


Figure 5-3. A2 Front Panel PCB Assembly

Table 5-4. A3 Timebase PCB Assembly
(See Figure 5-4.)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
C 1		CAP,VAR,1.5-14PF,250V,AIR	543520	51406	MVM014S	1	
C 2		CAP,CER,22PF,+-5%,50V,C0G	448449	71590	R220G13C0GHWFAP	1	
C 3		CAP,CER,0.01UF,+-20%,100V,X7R	407361	04222	3419-1000-103M	1	
C 4		CAP,CER,0.22UF,+-20%,50V,Z5U	309849	31433	C330C224M5U5CA	1	
J 1- 5		PIN,SINGLE,PWB,0.025 SQ	379438	00779	1-87022-0	5	
L 1		CHOKE,6TURN	320911	89536	320911	1	
R 1		RES,MF,47.5,+-1%,0.125W,100PPM	306076	91637	CMF5547R5F T-1	1	
R 2, 4- 7		RES,CC,560,+-10%,0.125W	115303	01121	BB5611	5	
R 3		RES,CC,1K,+-10%,0.125W	153916	01121	BB1021	1	
U 1	*	IC,ECL,DUAL 4-5 INPUT OR-NOR GATE	454967	04713	MC10109P	1	
Y 1		CRYSTAL,10MHZ,+-0.001%,HC-18/U	385732	61429	FLUKE 385732	1	

An * in 'S' column indicates a static-sensitive part.



7220A-1609

Figure 5-4. A3 Timebase PCB Assembly

MANUFACTURER'S FEDERAL SUPPLY CODES

00779
AMP, Inc.
Harrisburg, PA

01121
Allen Bradley Co
Milwaukee, WI

01295
TX Instruments, Inc.
Semiconductor Group
Dallas, TX

02735
RCA Corporation
Solid State Div.
Somerville, NJ

04222
AVX Corp.
AVX Ceramics Div.
Myrtle Beach, SC

04713
Motorola Inc.
Semiconductor Group
Phoenix, AZ

05397
Union Carbide Corp.
Materials Systems Div.
Cleveland, OH

06383
Panduit Corp.
Tinley Park, IL

07047
Ross Milton Co., The
Southampton, PA

07263
Fairchild Semiconductor
North American Sales
Ridgeview, CT

07910
Teledyne Semiconductor
Mountain View, CA

09023
Cornell-Dublier Electronics
Fuquay-Varina, NC

09214
General Electric Co
Semiconductor Products Dept
Auburn, NY

12040
National Semiconductor Corp
Danbury, CT

12697
Clarostat Mfg. Co., Inc
Dover, NH

14552
Microsemi Corp.
Santa Ana, CA

14936
General Instrument Co.
Discrete Semi Conductor Div
Hicksville, NY

15801
Fennel Electronics Inc.
Div. of Kidde Inc.
Framingham, MA

17856
Siliconix Inc.
Santa Clara, CA

18324
Signetics Corp.
Sacramento, CA

19701
Mepco/Centralab Inc.
N. American Philips Co.
Mineral Wells, TX

2K262
Boyd Corporation
Portland, OR

22526
Dupont, El DeNemours & Co.
Dupont Connector Systems
Advanced Products Division
New Cumberland, PA

24931
Specialty Connector Co.
Greenwood, IN

27014
National Semiconductor Corp.
Santa Clara, CA

28213
MN Mining & Mfg. Co.
Consumer Products Div.
3M Center
Saint Paul, MN

28480
Hewlett Packard Co.
Corporate HQ
Palo Alto, CA

30800
General Instrument Corp.
Capacitor Division
Hicksville, NY

31433
Kemet Electronics Corp.
Simpsonville, NC

32559
Bivar
Santa Ana, CA

32719
Siltronics
Santa Ana, CA

32997
Bourns Inc.
Trimpot Div.
Riverside, CA

51406
Murata Erie, No. America Inc.
(Also see 72982)

52500
Amphenol, RF Operations
Burlington, MA

54590
RCA Corp.
Electronic Components Div.
Cherry Hill, NJ

55261
LSI Computer Systems Inc.
Melville, NY

55285
Bercquist Company
Minneapolis, MN

56289
Sprague Electric Co
North Adams, MA

57053
Gates Energy Products
Denver, CO

57668
R-ohm Corporation
Irvine, CA

59124
KOA-Speer Electronics Inc.
Bradford, PA

59660
Tusonix Inc.
Tucson, AZ

60496
Micrel Inc.
Sunnyvale, CA

60705
Cera-Mite Corp.
Grafton, WI

61429
Fox Electronics
Cape Coral, FL

61529
Aromat Corporation
New Providence, NJ

61935
Schurter Inc.
Petaluma, CA

62643
United Chemicon
Rosemont, IL

65940
Rohm Corp & Whatney
Irvine, CA

MANUFACTURER'S FEDERAL SUPPLY CODES

70903
Cooper-Belden Corp.
Geneva, IL

71400
Bussman Manufacturing
Div. McGraw-Edison Co.
St. Louis, MO

71590
Mepco/Centralab
North American Philips Co.
Fort Dodge, IA

72982
Erie Specialty Products, Inc.
Erie, PA

74970
Johnson E F Co.
Waseca, MN

75915
Littelfuse Tracor
(Formerly: Tracor-Littelfuse)
Des Plaines, IL

79963
Zierick Mfg. Corp.
Mount Kisco, NY

80031
Mepco/Electra Inc.
Morristown, NJ

80294
Bourns Instruments Inc.
Riverside, CA

82389
Switchcraft Inc.
Sub of Raytheon Co.
Chicago, IL

88245
Winchester Electronics
Litton Systems-Useco Div.
Van Nuys, CA

89536
John Fluke Mfg. Co., Inc.
Everett, WA

9W423
Amatom
El Mont, CA

91506
Augat Alcoswitch
North Andover, MA

91637
Dale Electronics, Inc
Columbus, NE

95146
Alco Electronic Products Inc.
Switch Division
North Andover, MA

98291
Sealectro Corporation
BICC Electronics
Trumbill, CT

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Fremont, CA 94538
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14180 East Evans Avenue
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Tel: (201) 599-9500

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Dallas, TX 75229
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Tel: 43 222-60101, x1388

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Scientific & Industrial Equip. Div
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Brussels
Tel: 32 2 525 6111

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Sao Paulo
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Tel: 57 232-4532

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Section 6
Option & Accessory Information

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6-1. INTRODUCTION

6-2. This section of the manual contains information about options and accessories available for use with the 7220A. Where applicable, these descriptions will include the same kind of information as presented in Sections 1-5 of this manual (specifications, installation, theory of operation, etc.). Schematic diagrams for any appropriate option or accessory may be found in Section 8.

6-3. Accessory information can be identified with "600-" paragraph numbers. For options, relevant page and paragraph numbers contain the option number.

Accessories

600-1. ACCESSORIES

600-2. Ordering Information

600-3. When appropriate, installation instructions are included with each accessory ordered. Be sure to include the accessory model number when ordering.

600-4. Rack and Panel Adapters

600-5. Mounting kits may be ordered to adapt the standard 7220A PTI-style size C instrument case to either rack or panel mounting. Each kit includes all mounting hardware. Model Y2014 allows one 7220A case to be mounted in a 19-inch rack, and Model Y2015 allows two 7220A cases to be mounted in a 19-inch rack. Model Y2020 allows one 7220A case to be panel-mounted.

600-6. Instrument Cables

600-7. Two instrument ribbon cables are available for connecting the Digital Interface Option -521 to the Interface PCB Assembly Option -522, which is mounted in the 1120A IEEE-488 Translator. The cables are identical in function and differ only in length. Cable Y7203 is 2 feet in length, and cable Y7204 is 5 feet in length. Cable Y7203 is supplied with Options -521 or -529.

600-8. Whip Antenna

600-9. The A53 Whip Antenna allows the 7220A to make RF measurements via the antenna rather than cable connection. The Whip Antenna attaches directly to the 7220A front panel Channel A or Channel B input BNC connectors, and can be swiveled or extended for easy positioning.

Table 600-1. 7220A Accessories

MODEL NO.	DESCRIPTION
Y2014	Single mount 19 inch rack
Y2015	Dual mount 19 inch rack
Y2020	Single mount panel
Y7203	2 foot connecting cable
Y7204	5 foot connecting cable
A53	Extendable whip antenna

Option -010
Battery Pack

010-1. INTRODUCTION

010-2. Option -010 is a nickel-cadmium rechargeable battery unit. The option uses "F" cell nicad batteries for a total capacity of 5.6 amp hours. With a completely discharged battery, charge time is a minimum of 16 hours at room temperature. A discharge cut-off relay has been incorporated to guard against discharging the nicads to too low a level. A thermistor sensor circuit monitors battery temperature and halts the charging if the battery gets too hot. The battery output is fused to protect it against short circuits. Housed in a separate plastic box to eliminate acid corrosion problems, the battery assembly is attached inside the top cover. This option can be installed in the field. Order kit number 72XXA-010K.

010-3. SPECIFICATIONS

010-4. Specifications for the -010 Battery Option are listed in Table 010-1.

010-5. INSTALLATION

010-6. Use the following procedure to install the -010 Battery Option. Refer to Figure 010-1 for installation instructions. Component location can also be determined using Figures 010-3 and 010-4.

1. Remove line power from the instrument.

2. Remove the top cover using the procedure described in Section 4.

3. Place the battery assembly so that the battery and Battery Option PCB are closer to the front of the instrument and the two instrument handle hold-down bolts are through the corresponding holes on the battery bracket.

4. Place the two nuts on the instrument handle hold-down bolts and tighten.

5. Remove the bottom cover using the procedure described in Section 4. Do not remove the Front or Rear Panel assemblies from the Main PCB.

6. Locate solder bridge SB1 near the BTRY/LINE switch on the bottom of the Main PCB. (For 7220A, SB1 is on the front left corner of the bottom of the main PCB). Remove the short. In addition, remove the short on SB6 for the 7261A only.

7. Install the bottom cover.

8. Plug the two cables from the Battery Option PCB into their appropriate connectors on the Main PCB. Grey plug to JB1, black plug to JB2.

9. Fasten the grey ribbon cable under the grey retaining clip (located on the bottom side of the instrument's top cover).

10. Install the top cover of the instrument.

Table 010-1. Specifications

Capacity	5.6 Ampere hours
Battery Type	Four size "F" nicad cells
Charge Time	16 hours minimum at room temperature
Charge Protection	Thermistor actuated shut down of charging circuit if battery gets near 65°C
Discharge Protection	Low voltage automatic shut down at about +4V to prevent battery discharging to a reversed cell condition.

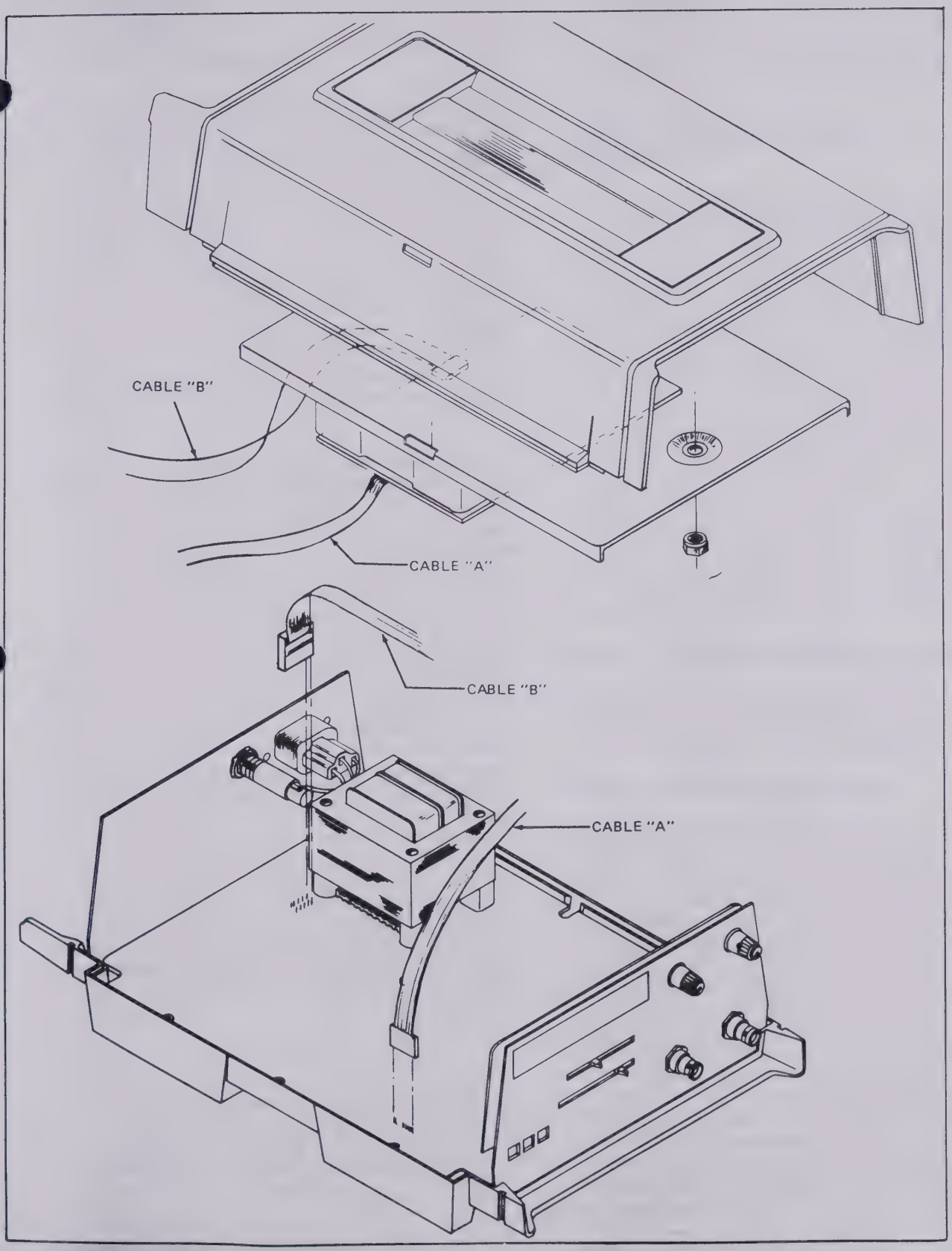


Figure 010-1. Installation

010-7. OPERATION

010-8. To use the battery for instrument power, set the BTRY/LINE switch to the BTRY position. The ON/STBY switch functions normally. The instrument may be powered from the battery with the line cord plugged into line power. This serves no useful purpose, however, and discharges the battery needlessly. When the battery has discharged to about 4V, the low battery voltage relay will remove the instrument load from the battery output, preventing the battery from discharging to too low a level. Place the two POWER switches in the STBY and LINE positions to recharge the battery. After the battery has been charged sufficiently, the RESET switch on the instrument front panel must be pressed to unlatch the low voltage relay and restore normal battery operation.

010-9. If neither oven time base option is installed, the battery will recharge any time the instrument is connected to line power and the power control is set to STBY. The charge rate is maximum when the ON/STBY switch is in the STBY position, and the BTRY/LINE switch is in the LINE position. If the battery is discharged completely, this charge rate will recharge the battery in 16 hours at temperatures around 22°C (72°F). If either oven time base is installed, the BTRY/LINE switch determines which source will power the oven. For maximum charge, the switch must be in the LINE position and the ON/STBY switch must be in the STBY position. If the BTRY/LINE switch is in the BTRY position and the ON/STBY switch is in the STBY position, the oven will draw about 200 mA of the 560 mA charging current. Under these conditions, the battery may not charge completely. If the POWER switches are in the ON and LINE positions, the charging rate will be reduced to prevent overheating inside the instrument. This charge rate is insufficient to recharge the battery but will maintain a float charge on the battery. The thermocouple sensor will halt the charge to keep the battery temperature from exceeding 65°C (149°F). (This will only occur in high ambient temperature environments.) The battery charge will automatically resume when the battery has cooled enough.

NOTE

Battery manufacturers recommend that nicad batteries should not be stored for extended periods of time without recharging at least every 90 days. Storage temperature below 25° C (77° F) is recommended.

010-10. THEORY OF OPERATION

010-11. The theory of operation for the -010 Option will be divided into a basic functional description of the major circuits of the option and a detailed circuit analysis of each circuit.

010-12. BASIC FUNCTIONAL DESCRIPTION

010-13. As Figure 010-2 shows, there are four main sections to the Battery Option PCB circuitry. The Current Source uses +5V unregulated power from the Main PCB to provide the charging current for the battery. The charging rate (high or low) is determined by the position of the ON/STBY switch. The Battery Hi-Temp Circuit reduces the charging current if the battery temperature approaches 65° C. The Low Battery Voltage Relay circuit normally passes the battery power on to the BTRY/LINE switch. Should the battery voltage drop to around 4V, the relay contacts will open, removing the load from the battery. The RESET switch on the instrument front panel must be pressed to restore the Low Battery Voltage Relay Circuit. If the BTRY/LINE switch is in the BTRY position, the +5V power from the battery is connected to the ON/STBY switch, and the oven if an oven time base is installed. If the ON/STBY switch is in the ON position, the battery power is supplied to the instrument and the Inverter circuit. The Inverter circuit provides operating voltages for the -5V, +12V and -12V regulators.

010-14. DETAILED CIRCUIT ANALYSIS

010-15. The Battery Option Schematic in Section 8 will be used to illustrate the detailed circuit analysis. The battery and thermistor are located inside the battery case.

010-16. Battery Hi-Temp Circuit

010-17. The Battery Hi-Temp Circuit is an inverting amplifier that protects the battery by reducing the battery charging current as the battery temperature approaches 65°C. It does this by altering the bias voltage of the Current Source controller to turn off the current source. The inverting amplifier is U1B with thermistor RT1 used as the feedback resistor. The positive input of the op amp is COMMON. The negative input is the -12V coupled through R9. RT1 is located next to the battery. When the battery is about 22°C, the resistance of RT1 will be about 50Ω. At this time, the output of the inverting amplifier (felt at the lower junction of R7 and R8) is about +.4V. RT1 exhibits a positive temperature coefficient. As the battery temperature rises, the resistance of RT1 increases. When the battery temperature approaches 65°C, the resistance of RT1 passes over a sharp knee and approaches 500Ω. The output of the negative gain amplifier approaches +5V.

010-18. Current Source

010-19. The Current Source uses the unregulated +5V from the Main PCB to provide charging current for the

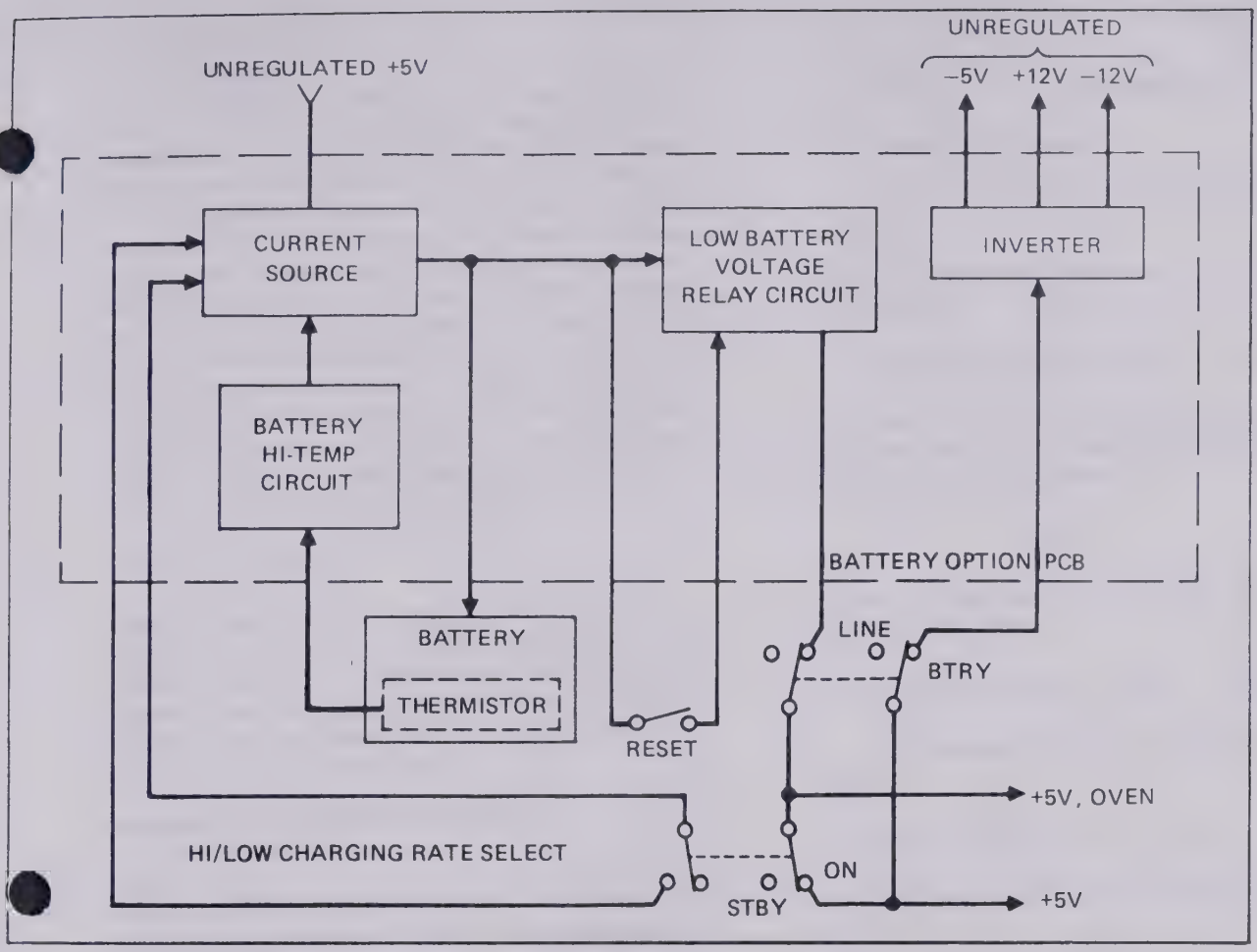


Figure 010-2. -010 Option Block Diagram

battery. This circuit consists of the series pass element, Q1; the sensing element, R1; the control element, U1A; and their associated circuitry. Q1 directly controls the current charging the battery. The base bias of Q1 is in turn controlled by the output of U1A. The positive input is battery voltage felt on the battery side of R1 (TP2). The negative input is picked off the voltage divider network composed of R2, R8 and sometimes R7. The voltage divider is between the input side of R1 (TP1) and the output of the Battery Hi-Temp circuit.

010-20. The charging current is changed by altering the input to U1A from the voltage divider. The voltage divided input is altered by changing the position of the ON/STBY switch. When the switch is in the STBY position, R7 is placed in parallel with R8. Their combined resistance is about one-fifth that of R8 alone. At normal operating temperatures, the bottom of the voltage divider is at +0.5V and the top is at battery voltage plus the voltage drop across R1. The op amp causes Q1 to pass n[illegible]ally 560 mA through R1. If the ON/STBY switch is i[illegible]e ON position, R7 is no longer in parallel with R8. This change in the voltage divider input to U1A will cause the charging current to decrease to nominally 110 mA. If the battery temperature approaches 65° C, the bottom of the voltage divider becomes +5V and the voltage at TP1 approaches the battery voltage. This decreases the output of the op amp cutting off Q1. As the battery cools, the resistance of the thermistor decreases allowing the battery charge to resume. If F1 blows, removing the regulated input to U1A, CR10 will limit the conduction of Q1 so that the voltage at TP2 does not exceed 6V.

010-21. Low Battery Voltage Relay Circuit

010-22. The low battery voltage relay keeps the battery from discharging to a reversed cell condition by removing the battery load when battery voltage drops to about 4V. The battery is connected to its load through K1, a two coil latching relay. During normal operation, the battery and its load are connected, Q2 and Q6 are off and Q5 is in saturation. When battery voltage drops to about 4V, the base bias on Q5 (TP5) is low enough to cut Q5 off. This lets the input on pin 13 of flip-flop U2 rise. This will

change the state of U2 making the output on pin 11 of U2 go low. This causes Q6 to conduct, charging C2 and turning Q2 on. When Q2 conducts, the coil of K1 in the collector of Q2 will energize, opening K1. When K1 removes the battery loads, the input circuitry for Q2 is deenergized. C2 has been charged to make Q2 conduct long enough to insure that K1 is latched in the open condition. After the battery has been recharged, pressing the RESET switch on the front panel will connect battery voltage to both the reset coil of K1 and pin 6 of U2. The RESET switch contacts will be closed long enough to insure that K1 will be latched shut. This will restore the connection between the battery and its load. Q5 will go into saturation. The battery voltage at pin 6 of U2 will cause pin 11 to go high, turning off Q6.

010-23. Inverter

010-24. The Inverter is composed of Q3, Q4, T1 and their associated circuitry. The three components form an oscillator that runs at about 10 kHz. This oscillation allows T1 to step up the battery voltage to provide rectified operating voltages to the -5V, +12V and -12V regulators for instrument power.

010-25. PERFORMANCE TEST

010-26. Use the following procedure as a performance test. Table 010-2 lists the test points. The component location diagram at the end of this option can be used to locate these test points. The instrument will be referred to as the UUT (Unit Under Test). Use a variable DC power supply with an output range of at least 3-5V and the test equipment listed in Section 4.

1. Remove the top cover of the UUT using the procedure given in Section 4. Leave the cables from the Battery Option PCB connected to the Main PCB and lay the top cover beside the instrument, upside-down. The grey ribbon cable will have to be removed from the retaining clip on the bottom side of the top cover.

Table 010-2. Test Points

TEST POINTS	COMMENTS
TP1, TP2	Voltage across sensing resistor, R1.
TP3	COMMON
TP4	Battery voltage.
TP5	Low Battery Voltage Sensing Point
TP6	Low Battery Voltage Cut-Off Signal.

2. Connect the UUT to line power.

3. On the UUT front panel:

   a. Set the ON/STBY switch to the STBY position.

   b. Set the BTRY/LINE switch to the LINE position.

4. Connect the DVM: + to TP2, - to TP3.

5. Verify that the DVM reads greater than 5V. If it does not, continue the charge until this reading (Battery Voltage) is at least 5V.

NOTE

In the next step, the DVM test leads must be isolated from ground.

6. Connect the DVM: + to TP1, - to TP2.

7. Verify that the DVM reads between 96 mV and 128 mV.

8. Set the ON/STBY switch to ON.

9. Verify that the DVM reads between 14 mV and 30 mV.

10. Set the ON/STBY switch to STBY.

11. Connect the DVM: + to TP4, - to TP3.

12. Verify that the DVM reads battery voltage. If there is no voltage present, press the RESET switch on the front panel. The DVM should now read battery voltage.

CAUTION

Counter must be disconnected from ground during the following soldering procedures. Disconnect the power cord and any other connection (e.g., BNC) that may be introducing a ground to the instrument.

13. Unsolder an end of the fuse wire located on the PCB near the battery harness.

14. Adjust the DC Power Supply for a +5V output.

15. Connect the DC Power Supply + to TP2, - to TP3.

16. Connect the DVM + lead to TP4, – lead to ground.

17. Slowly reduce the DC Power Supply voltage until the relay opens as indicated by the voltage of TP4 dropping suddenly to 0V. (The click of the relay may also be heard.)

18. Verify that the output voltage of the DC Power Supply is between +3.8V and +4.3V.

19. Disconnect the DC Power Supply. Resolder the fuse wire.

20. On the front panel of the UUT:

a. Press and release the RESET switch.

b. Set the ON/STBY switch to the ON position.

c. Set BTRY/LINE switch to the BTRY position.

d. Set the RESOLUTION switch to the 1 kHz position. (For 7220A, 100 Hz.)

e. Set the function select switch to the CHK position.

21. Verify that the UUT display reads 10.000. (For 7220A, display should read 10.0000.)

010-27. MAINTENANCE

010-28. Battery Replacement

010-29. Use the following procedure to replace the battery:

1. Remove the line power from the instrument.

2. Remove the top cover of the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Disconnect the two cables between the Battery PCB and the Main PCB.

4. Remove the four screws holding the battery case to the battery bracket.

5. Note the position of the thermistor. This will be important in a later step.

6. Lift the battery case and Battery Option PCB off the battery and place it to one side.

7. Unsolder the two wires connected to the battery (white and black).

8. Dispose of the old battery.

9. Solder the white and black wires to the tabs on the new battery. White to the tab on the recessed battery end (+) and black to the tab on the flush battery end (–).

10. Replace the battery case being sure to place the thermistor in the same position noted in step 5.

11. Connect the two cables between the Battery PCB and the Main PCB.

12. Replace the top cover.

010-30. Fuse Replacement

010-31. Use the following procedure to replace the fuse on the Battery Option PCB:

1. Remove the line power from the instrument.

2. Remove the top cover from the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Unsolder the ends of F1 from its terminals.

4. Solder a suitable length of #35 magnet wire between the fuse terminals.

5. Place the top cover on the instrument.

010-32. LIST OF REPLACEABLE PARTS

010-33. Table 010-3 is a list of replaceable parts for the battery assembly. Figure 010-3 is the component location diagram for this table.

Table 010-3. Battery Assembly (Option -010)
(See Figure 010-3.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
BT 1		BATTERY,NI-CAD,5.0V,5.6AH	484048	57053	41B042AE00301	1	
C 1, 4, 7-		CAP,TA,2.2UF,+-20%,20V	161927	56289	196D224X0020HA1	6	
C 10			161927				
C 2		CAP,TA,4.7UF,+-20%,25V	161943	56289	196D475X0025KA1	1	
C 3		CAP,TA,330UF,+-10%,6V	193011	31433	T310D337K006AS	1	
C 5		CAP,CER,47PF,+-20%,1000V,C0G	369132	60705	561CC0GCK102EG470M	1	
C 6		CAP,CER,0.1UF,+80-20%,25V,Z5U	369199	19701	U104M59Y5PEGTKM	1	
CR 1- 9	*	DIODE,SI,BV=75V,IO=150MA,500MW	203323	07910	1N4448	9	
E 1- 6		TERM,UNINSUL,STANDOFF,TURRET	208355	88245	2060B6	6	
H 1		SCREW,MACH,PH,P,STL,4-40X0.375	152124	COMMERCIAL		2	
H 2		NUT,HEX,S.STL,4-40	147611	COMMERCIAL		2	
H 3		WASHER,LOCK,INTRNL,STEEL,#4	110403	COMMERCIAL		2	
H 4		SPACER,TRANSISTOR MOUNT,DAP,TO-5	152207	07047	10123-DAP	1	
H 5		SPACER,SWAGED,RND,SS,6-32,.250	500074	9W423	9533B-SS-0632	4	
H 6		WASHER,LOCK,INTRNL,STEEL,#6	110338	COMMERCIAL		4	
H 7		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		8	
H 8		SCREW,MACH,PH,P,STL,4-40X0.250	129890	COMMERCIAL		1	
H 9		WASHER,SHLDR,NYLON,.113,.245	485417	COMMERCIAL		1	
H 10		WASHER,LOCK,SPLIT,STEEL,#4	110395	COMMERCIAL		1	
H 11		WASHER,FLAT,FIBER,#6,0.047 THK	246488	COMMERCIAL		4	
H 12		WASHER,FLAT,STL,.170,.375,.031	110288	COMMERCIAL		4	
H 13		SPACER,RND,SOLUBLE,.156OD,.060THK	296319	32559	TO-8-06	1	
K 1		RELAY,ARMATURE,2 FORM C,5VDC	484535	61529	NC2D-JPL2-5VDC	1	
L 1		CHOKE	502138	89536	502138	1	
MP 1		SOCKET ACC,POLARIZING KEY	500801	28213	3433-0000	1	
MP 2		BATTERY CASE F-CELL	475459	89536	475459	1	
MP 3		BATTERY PACK BRACKET	476200	89536	476200	1	
MP 4		INSUL PART,TRANS,PLASTIC,TO-220,FILM	412809	13103	43-77-8	1	
MP 5		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
Q 1	*	TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	09214	D44C5	1	
Q 2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	346916	07263	2N2219A	1	
Q 3, 4	*	TRANSISTOR,SI,BV=70V,90W,TO-127	325720	04713	MJE3055	2	
Q 5	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	
Q 6	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	04713	2N3906	1	
R 1		RES,WW,.2,+-3%,.7W	255661	05347	MS30R2H	1	
R 2		RES,MF,1.1K,+-1%,0.125W,100PPM	241497	91637	MFF1-81101F	1	
R 4		RES,CF,100K,+-5%,0.25W	348920	80031	1-4-5P100K	1	
R 5		RES,MF,86.6K,+-1%,0.125W,100PPM	291468	91637	CMF558662F T-1	1	
R 6, 10		RES,CF,47,+-5%,0.25W	441592	80031	1-4-5P47E	2	
R 7		RES,MF,61.9K,+-1%,0.125W,100PPM	237230	91637	CMF-55 6192 F T-1	1	
R 8		RES,MF,249K,+-1%,0.125W,100PPM	268805	91637	CMF552493F T-1	1	
R 9		RES,CF,1.2K,+-5%,0.25W	441378	80031	1-4-5P1K2	1	
R 11		RES,CC,10,+-5%,1W	166298	01121	GB1005	1	
R 12		RES,CF,330,+-5%,0.25W	368720	80031	1-4-5P330E	1	
R 13		RES,CF,82,+-5%,0.25W	442277	80031	1-4-5P82E	1	
R 14		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F T-1	1	
R 15		RES,MF,6.65K,+-1%,0.125W,100PPM	294918	91637	CMF-55 6651 F T-1	1	
R 17		RES,CF,1K,+-5%,0.25W	343426	59124	CF1-4 102 J B	1	
R 18		RES,CF,470,+-5%,0.25W	343434	80031	1-4-5P470E	1	
RT 16		THERMISTOR,DISC,NEG.,10K,+-10%,25C	104596	15801	JA41J1	1	
T 1		TRANSFORMER INVERTER	486530	89536	486530	1	
U 1	*	IC,OP AMP,SELECTED DIFF OUT VOLT=2MV	473777	27014	SL62516	1	
U 2	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	04713	MC14001BCP	1	
VR 10	*	ZENER,UNCOMP,7.5V,5%,20.0MA,0.4W	256446	14552	1N755A	1	
W 1		BATTERY CABLE 1	488403	89536	488403	1	
W 2		BATTERY CABLE 2	488411	89536	488411	1	
W 3		ASSY BATTERY CABLE III	491704	89536	491704	1	

An * in 'S' column indicates a static-sensitive part.

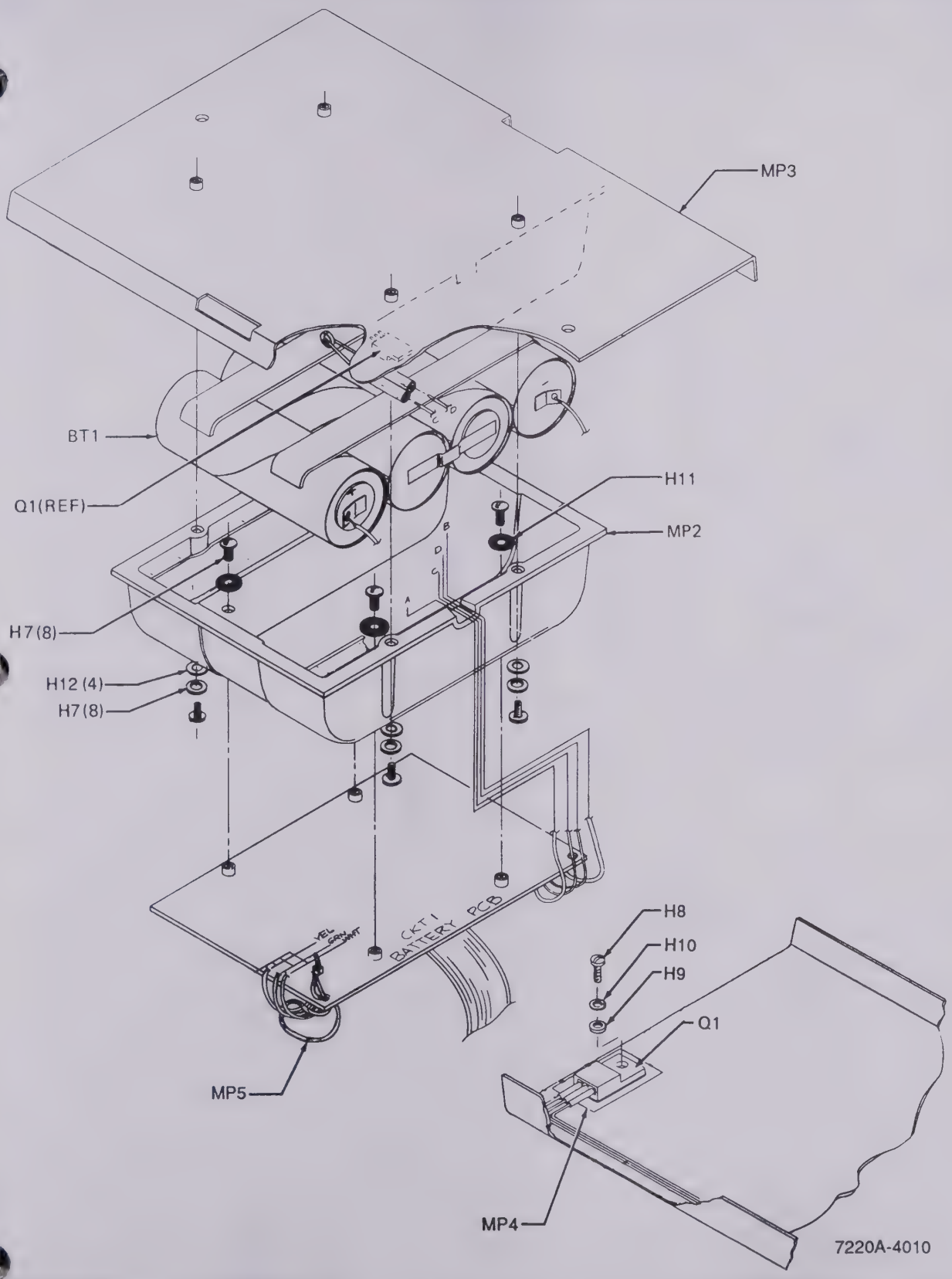


Figure 010-3. Battery Assembly Option -010

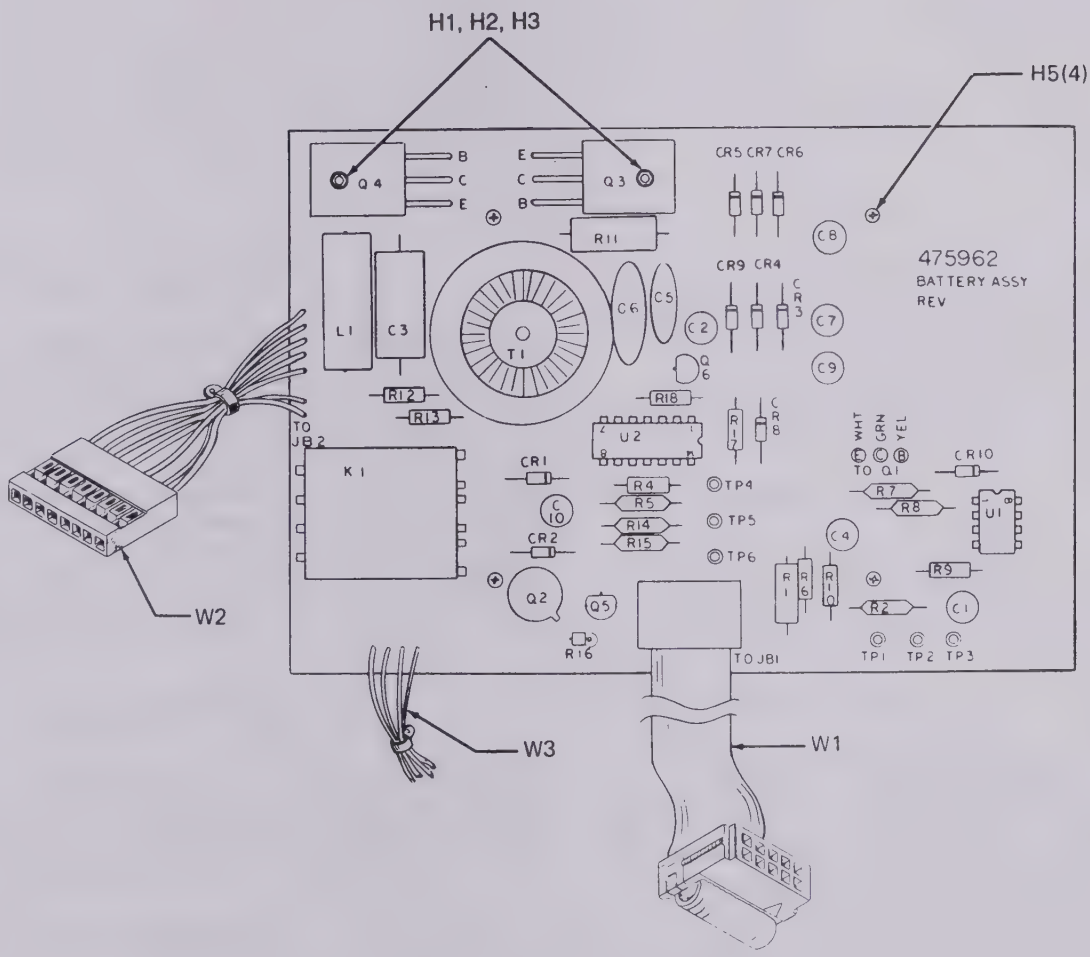


Figure 010-3. Battery Assembly Option -010 (cont)

Option-111
1 PPM TCXO

111-1. INTRODUCTION

111-2. Option -111 is a temperature compensated crystal oscillator (TCXO) with an intrinsic stability greater than the standard time base. This increased stability is due to a temperature compensation network. Figure 111-1 shows the frequency variation for change in temperature for an uncompensated oscillator and the compensation network effect. The resulting frequency deviation (solid line) is held to a minimum over the designated temperature range. If the temperature limits are exceeded, the time base stability may exceed the specified value.

111-3. SPECIFICATIONS

111-4. Specifications of the 7220A-111 Option are listed in Table 111-1. Comparative specifications for the other time bases available are listed in Section 1 of the 7220A Instruction Manual.

111-5. INSTALLATION

111-6. Installation of the 1 PPM TCXO (Option -111) necessitates removal of the counter's Main PCB; refer to disassembly instructions in Section 4 of the Instruction Manual. The TCXO is installed in the left rear corner of the Main PCB. Use the following procedure:

1. Unsolder and remove any other time base already installed.

2. Refer to Figure 111-2 and install the insulator and the TCXO.

3. While exercising care not to overheat the Main PCB, solder the TCXO connections.

4. Complete the following jumper and solder bridge arrangements as follows: If necessary, remove the short at SB2 (bottom of Main PCB, front left corner). Also, if necessary, remove the short at SB4 or SB5 (bottom of Main PCB, left rear corner). Solder a jumper at SB3 (left rear corner).

111-7. OPERATION

111-8. Operation of the instrument with the Option -111 installed is the same as operation of a standard instrument. Refer to Section 2 for operating instructions.

111-9. CALIBRATION

111-10. Calibration for the TCXO (Option -111) time base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{-9}$. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz Resolution setting on the counter, this method yields an adjustable accuracy of +5 parts in 10^8 ($\pm$ one count error). Proceed with the following steps:

1. Remove the top cover from the 7220A.

2. Press the POWER switch to ON. Allow a minimum warmup of twenty minutes.

WARNING

LINE VOLTAGE IS PRESENT WHENEVER POWER CORD IS CONNECTED.

3. Apply an external frequency source of 10 MHz (100 mV rms) with an accuracy of $\pm 1 \times 10^{-9}$

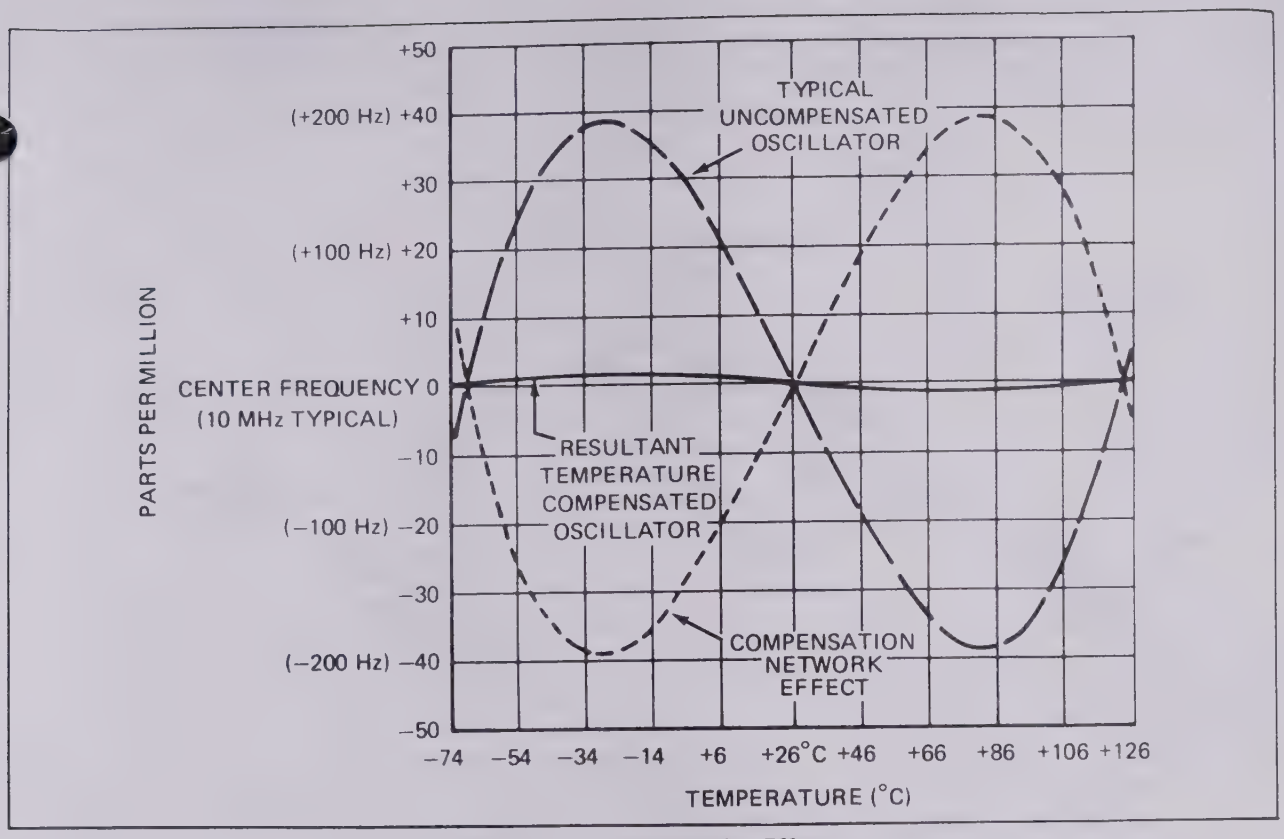


Figure 111-1. Compensation Effects

4. On the 7220A front panel, make the following settings:

RESOLUTION	1 Hz
CH A/CH B	125 MHz
ATTENUATION	as required for a stable display

5. Ascertain the offset frequency for the installed 1 PPM TCXO. This figure is stamped on the TCXO case (which is mounted on the left rear corner of the Main PCB).

Table 111-1. Option 7220A-111 Specifications

Nominal Frequency		10 MHz
Aging Rate	per day	–
	per month	$\pm 3 \times 10^{-7}$
	per year	$\pm 1 \times 10^{-6}$
Accuracy with Temperature* (0° to 40°C)		$\pm 1 \times 10^{-6}$
Line Voltage (10% line variation)		$\pm 2 \times 10^{-7}$
Battery Operation		$\pm 2 \times 10^{-7}$

**Includes errors caused by temperature variations during operation as well as all calibration errors when calibrated per specifications.*

6. Locate the OPT. -111 FREQ ADJ port on the lower right corner of 7220A rear panel.

7. Using a non-ferrous alignment tool (Fluke Part Number 542886, Fed. Stock 5120-724-3767), adjust the 1 PPM TCXO through the access port. Adjust for a displayed reading of 10.000000 MHz MINUS the offset frequency. For example, with an offset stamped on the TCXO of -3.7 Hz, adjust for a display of 10.000004 MHz.

8. Set the RESOLUTION control to 0.1 Hz.

9. Now adjust the TCXO for a displayed reading of 10.0000000 MHz MINUS the offset frequency For the example given in Step 7, the display should be 10.0000037 Hz.

10. Install the 7220A top cover.

111-11. REPLACEABLE PARTS

111-12. The 7220A Option -111 1 PPM Oscillator is a completely sealed unit containing no replacement parts. However, the 7220A-111 Option Kit (Fluke Part Number 575100) does include the -111 PPM Oscillator (Fluke Part Number 516104) and the Insulator (Fluke Part Number 487710), either of which may be ordered separately. For information about ordering, see Section 5.

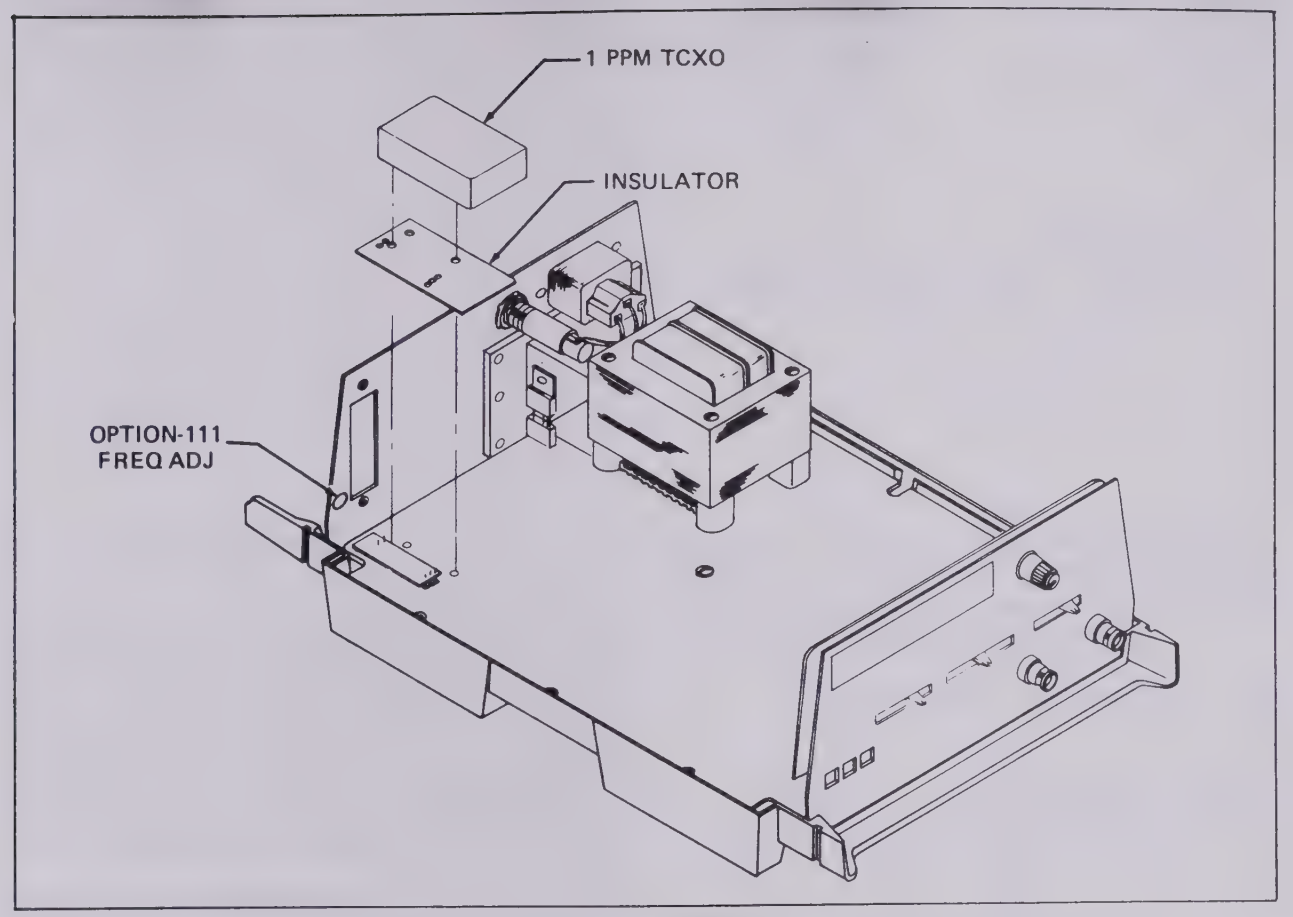


Figure 111-2. Installation

Option-131
Low Power Oven Time Base

131-1. INTRODUCTION

131-2. The -131 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -131 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

131-3. SPECIFICATIONS

131-4. The specifications of the -131 Option are listed in Table 131-1.

131-5. INSTALLATION

6131-6. Installation of the Low Power Oven Time Base (Option -131) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 131-1, install the Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as described below:

a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 131-1. -131 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	1×10^{-7}/month*
Accuracy with Temperature (0° to 40°C)	$\pm 1 \times 10^{-7}$
Line Voltage (10% line variation)	2×10^{-8}
Warmup**	
10 minutes	5×10^{-7}
20 minutes	3×10^{-8}
Battery Operation	$\pm 5 \times 10^{-8}$

* After 5 days continuous operation.

** Specifies offset from final frequency value (the value after 24 hours).

131-7. CALIBRATION

131-8. Calibration for the Low Power Oven Time Base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{-9}$. A cesium standard, such as the HP

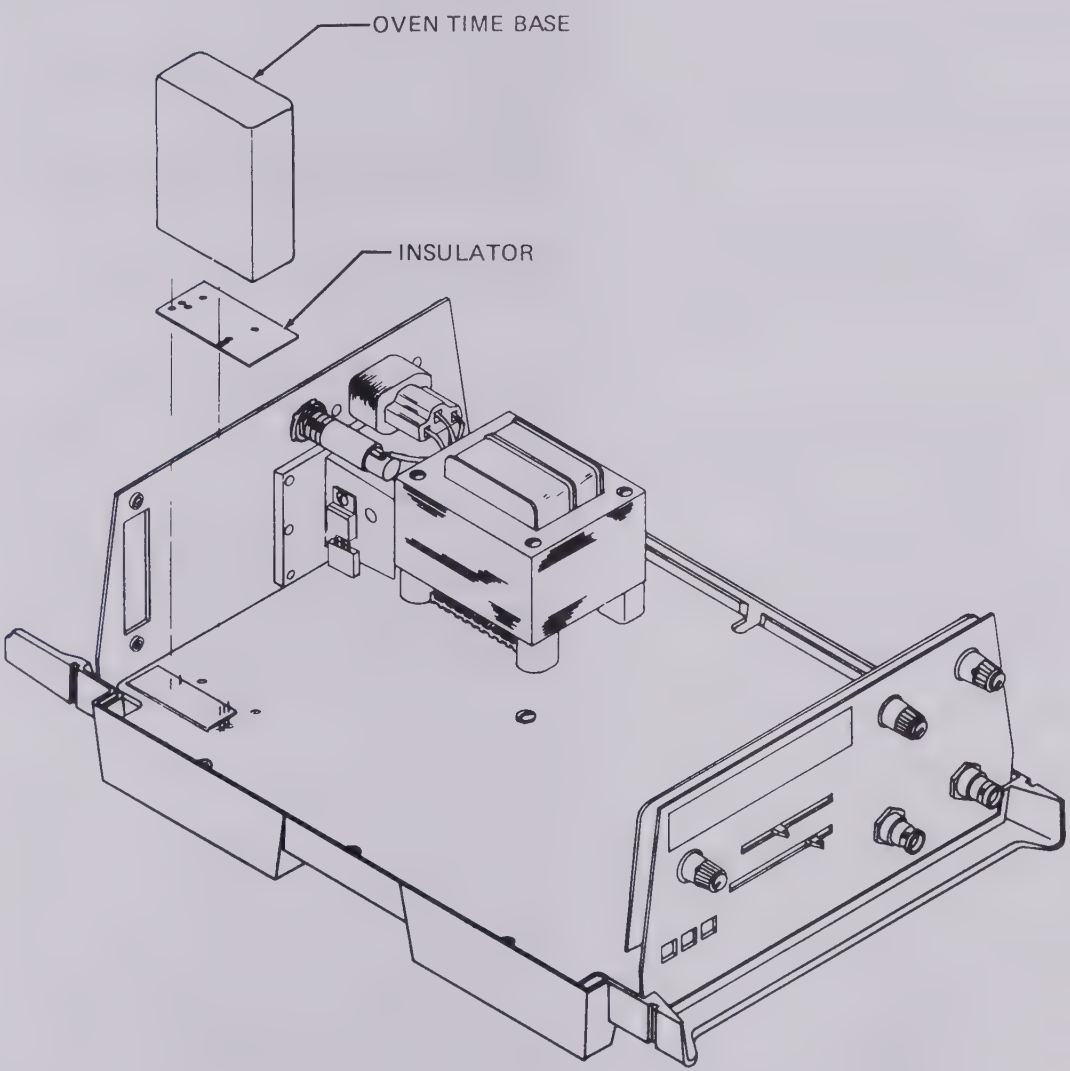


Figure 131-2. Installation

5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields an adjustable accuracy of 2 parts in 10^8 (± one count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6131-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6131-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds.

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

6131-9. LIST OF REPLACEABLE PARTS

131-10. A replacement oscillator can be ordered by using Fluke Part Number 516112. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 516112. The insulator can be ordered with part number 487710. Refer to Section 5 for ordering information.

Table 131-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

Option -132
Superior Low Power Oven Time Base

132-1. INTRODUCTION

132-2. The -132 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -132 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

132-3. SPECIFICATIONS

132-4. The specifications of the -132 Option are listed in Table 132-1.

132-5. INSTALLATION

132-6. Installation of the Superior Low Power Oven Time Base (Option -132) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Superior Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to figure 132-1, install the Superior Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as described below:

a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 132-1. -132 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	$\pm 3 \times 10^{-9}$/day*
	$\pm 5 \times 10^{-8}$/month*
Accuracy with Temperature (0° to 40°C)	$\pm 3 \times 10^{-8}$
Line Voltage (10% line variation)	$\pm 4 \times 10^{-9}$
Warmup	
10 minutes	$\pm 5 \times 10^{-7}$
20 minutes	$\pm 3 \times 10^{-8}$
Battery Operation	$\pm 1 \times 10^{-8}$

* After 5 days continuous operation.

** Specifies offset from final frequency value (the value after 24 hours).

132-7. CALIBRATION

132-8. Calibration for the Superior Low Power Oven Time Base necessitates the use of a frequency reference

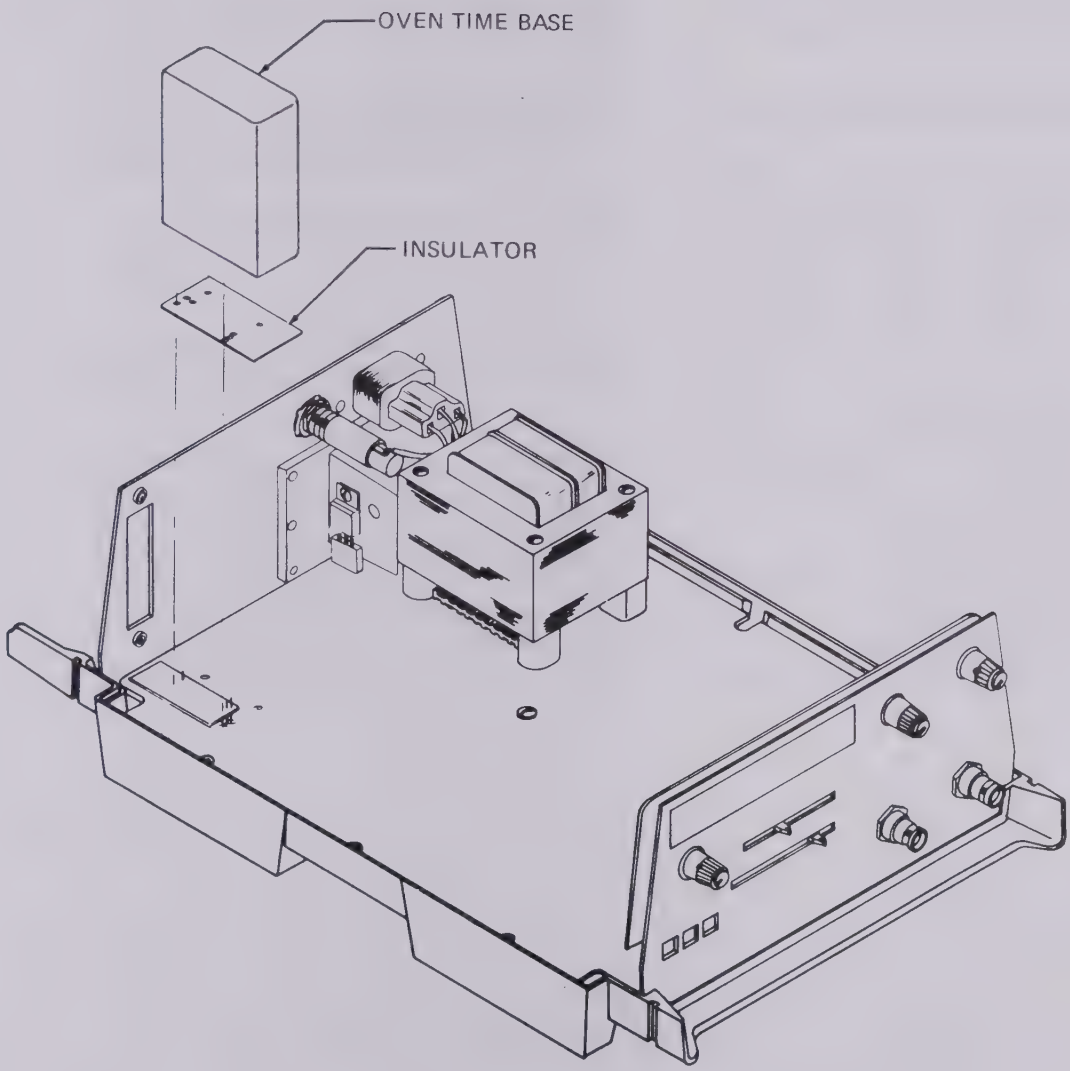


Figure 132-1. Installation

with an accuracy of ±1 X 10^9. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields an adjustable accuracy of 2 parts in 10^8 (±1 count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 132-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) nonferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 132-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

132-9. LIST OF REPLACEABLE PARTS

132-10. A replacement oscillator can be ordered by using the Fluke Part Number 516096. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 516096. The insulator can be ordered with Fluke Part Number 487710. Ordering information is given in Section 5 of the Instruction Manual.

Table 6132-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

Option -351
Resolution Multiplier

351-1. INTRODUCTION

351-2. The Resolution Multiplier Option -351 is used to provide high resolution for low frequency Channel A input signals. This is accomplished by using a phase-locked loop to multiply the conditioned signals by a factor of 1000 before they are counted. This has the effect of increasing the four available Resolution settings by the same factor of 1000. When installed, the Resolution Multiplier may be selected by the 7220A front panel Function slide switch. The Resolution settings available in the Resolution Multiplier mode are color coded by the blue band on the front panel. When the Resolution Multiplier mode is not selected by the CH A/CH B slide switch, power is removed from the circuit.

351-3. SPECIFICATIONS

351-4. The specifications for the Resolution Multiplier Option -351 are given in Table 351-1.

Table 351-1. Specifications

7220A Input: Channel A					
Operating Range: 10 Hz to 10 kHz					
7220A Resolution with Option -351:	(Hz)	0.1	0.01	0.001	0.0001
Gate Time:	(sec)	0.01	0.1	1	10
Accuracy: ±2 counts ± timebase accuracy with signal input = 100mV RMS.					

351-5. INSTALLATION

351-6. Use the following procedure to install the Option -351:

1. Release the POWER switch to STBY and remove the line power cord. Remove the top cover. Remember that the case bottom is secured to the Main PCB Assembly with one central screw. Prying the case top up while pressing down on the case bottom may damage the Main PCB.

2. Referring to Figure 351-1, orient the Option -351 PCB so the components are facing the front, and gently guide the PCB down over the two alignment rods mounted on the Main PCB so that the eight connector pins on the Main PCB are properly inserted into the eight connectors on the Option -351 PCB. Firmly push the Option -351 PCB until it is securely connected to the Main PCB.

3. Reconnect the top case half, making sure that the Front and Rear panels fit into their appropriate grooves in the case top half. Slide the top half into place uniformly. Firmly squeeze top and bottom together (at front and rear), and reinstall the six securing screws.

NOTE

Proper RFI shielding depends on top and bottom case halves being securely mated.

351-7. OPERATION

351-8. The Resolution Multiplier may only be used with Channel A signal inputs, and its operating range is 10 Hz to 10 kHz. As can be seen in the Specification Table, the Resolution Multiplier can be used to increase the measurement resolution for the same gate times as without the Resolution Multiplier. For example, without Option -351 the gate time for the 0.1 Hz resolution is 10 seconds, whereas with the Option -351, the same 10 second gate time allows 0.0001 Hz resolution.

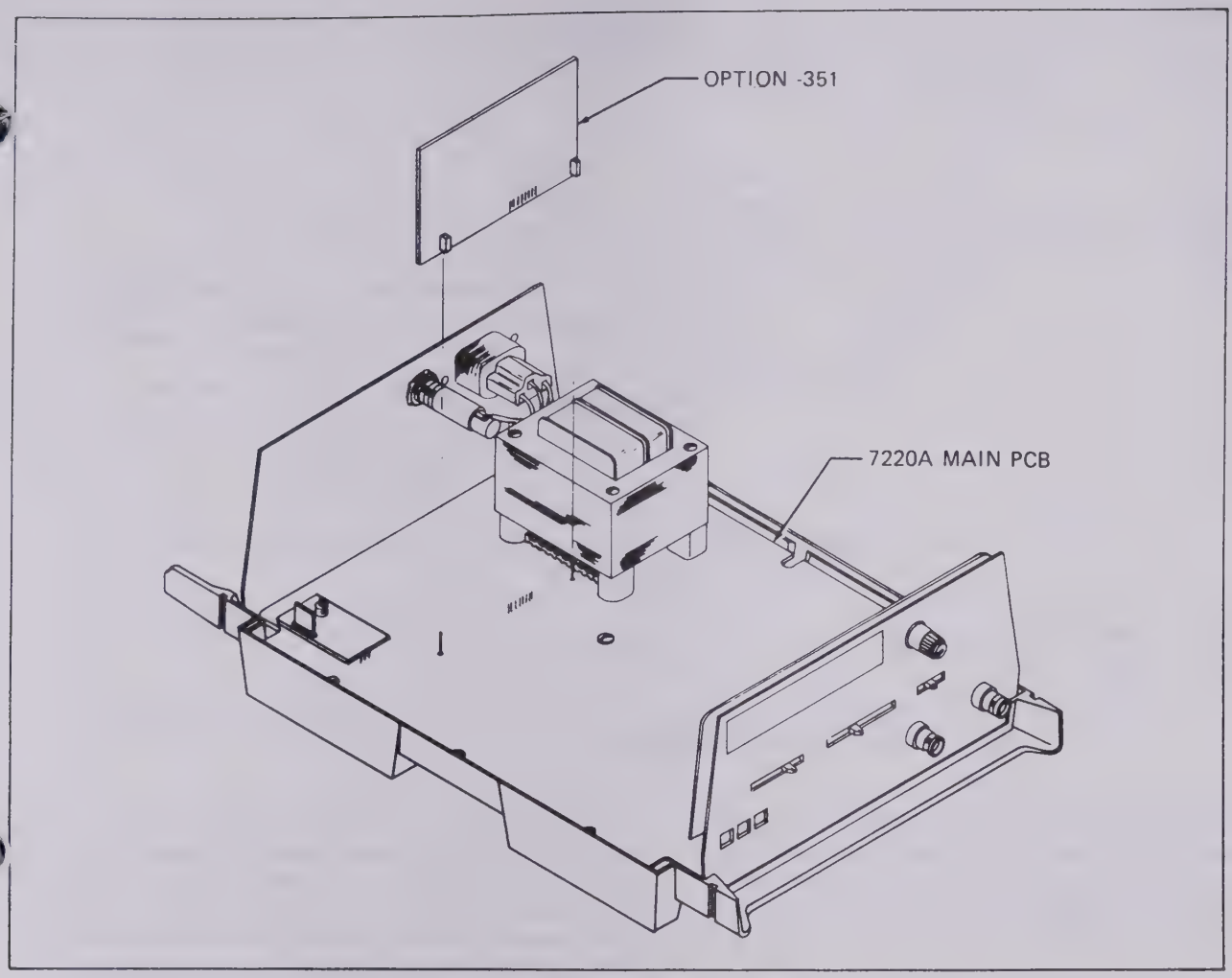


Figure 351-1. Option -351 Installation

351-9. The Resolution Multiplier can also be used to speed up measurement cycles by selecting shorter gate times. For example, a low frequency signal being measured with a resolution of 0.1 Hz requires a gate time of ten seconds. To adjust the frequency of the signal being measured while observing the counter would be very difficult because of the time lag between the adjustment and the resultant display on the counter. This problem can be solved with the Resolution Multiplier by selecting the 0.1 Hz or 0.01 Hz resolution settings, which have fast gate times of only 0.01 second or 0.1 second, thus decreasing the time lag to an acceptable amount.

351-10. To operate the counter with the Resolution Multiplier, proceed as follows:

1. Connect a 10 Hz to 10 kHz input signal to the Channel A front panel BNC connector.

2. Set the front panel CH A/CH B switch to RES MULT.

3. Select the desired resolution. The LED Gate annunciator at far left of the display will flash at the beginning of each gate time. The unit of measurement for the frequency on the display will be Hz.

351-11. THEORY OF OPERATION

351-12. The operation of the Resolution Multiplier is illustrated in Figure 351-2. The heart of the circuit is the frequency phase comparator U2 and the voltage controlled oscillator (VCO) Q6. The frequency phase comparator provides a feedback loop to maintain the precise dc voltage level needed for the VCO to oscillate at a frequency 1000 times the signal input.

351-13. As can be seen in Figure 351-2, the input signal from the Channel A preamp enters one input of the phase comparator. The second input to the comparator receives the actual output of the multiplier circuit after being divided by a factor of 1000. When the output of the

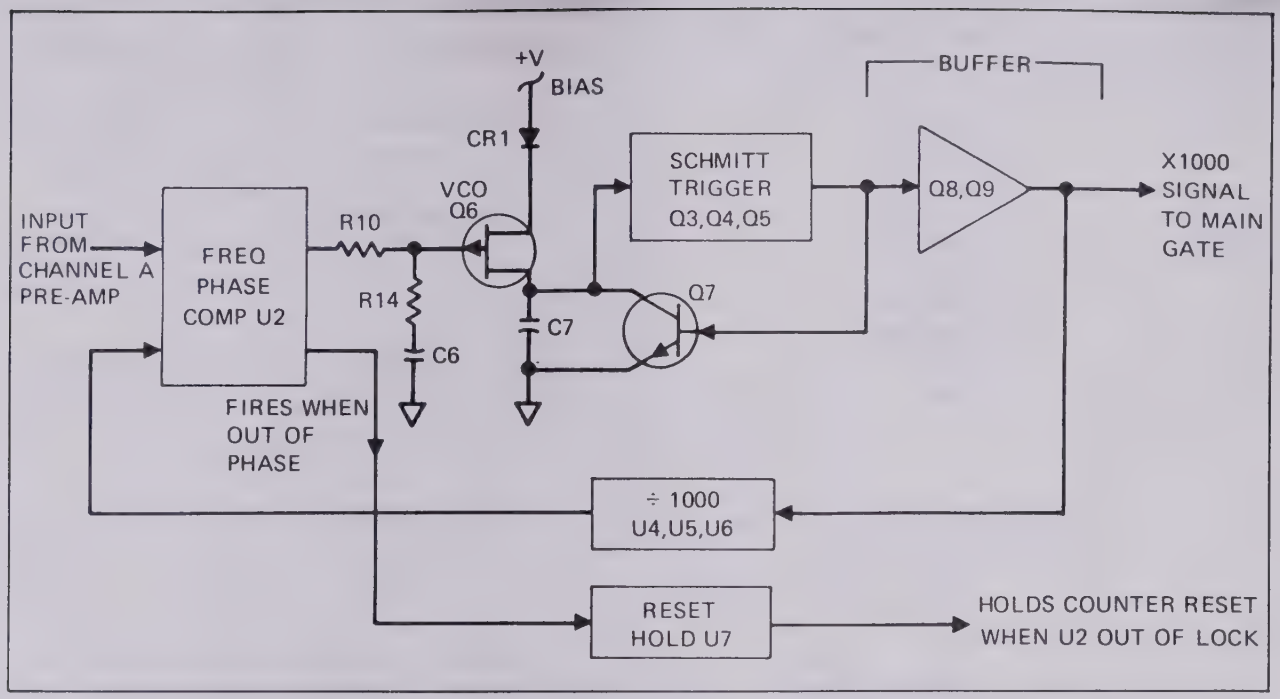


Figure 351-2. Resolution Multiplier Circuit

multiplier is exactly 1000 times greater than the input from the preamp, the two comparator inputs are in phase and a constant dc level is present at the VCO input. The comparator output, filtered by R10, R14, and C6, drives Q6 and controls the charging rate of C7 through CR1. The voltage across C7 is applied to the input of a Schmitt trigger (which changes state at some threshold point). The Schmitt trigger causes Q7 to discharge C7 to begin the action again.

351-14. The output of the Schmitt trigger is buffered by Q8 and Q9 (NPN type) and fed to the Main Gate for counting. The output is also divided by 1000 and fed back for comparison with the input from the Channel A preamp to form the phase-locked loop. Any frequency or phase difference between the two inputs will cause the output dc level applied to the VCO to change to maintain multiplied output equal to 1000 times the input. Whenever the multiplier is not locked in phase, it triggers the timer U7, which generates the reset pulse that resets the counters. This holds off the counter during start-up or when an invalid input is present at the multiplier.

351-15. PERFORMANCE CHECK

351-16. The following procedure can be used to check whether the installed Resolution Multiplier Option -351 is functioning properly. It is assumed when following this procedure that the 7220A is functioning properly and within the instrument specifications listed in Section 1 of the Instruction Manual. If the 7220A Option -351 fails to satisfy the requirements of this performance check, refer to Section 4 of the Instruction Manual and verify that the 7220A satisfies the requirements for the instrument performance test (Channel B does not need to be tested, since it is not used in the Resolution Multiplier mode).

351-17. A low frequency signal source is needed for this procedure. The Fluke 6011A is recommended.

1. Set the 7220A CH A/CH B slide switch to RES MULT. Be sure the rear panel REF switch is set to INT.

2. Connect the low frequency signal source to the 7220A Channel A input. Set the input frequency to 100 Hz at 20 mV rms.

3. Set the 7220A RESOLUTION to .0001 Hz and confirm that the resultant display is as listed in Table 351-2.

4. Repeat Step 3 for the next three RESOLUTION settings in Table 351-2.

5. Set the RESOLUTION to .001 Hz and set the input signal to 10 Hz at 20 mV rms. Confirm that the display is as listed in Table 351-2. Repeat this for the next three input signals listed.

6. Set the input signal to 25 kHz at 20 mV rms and confirm the display is as listed. The GATE LED

Table 351-2. Option -351 Display

RESOLUTION	INPUT SIGNAL	CORRECT DISPLAY (±2 counts ± timebase accuracy)
.0001 Hz	100 Hz (20 mV rms)	100.0000 Hz
.001 Hz	100 Hz "	100.000 Hz
.01 Hz	100 Hz "	100.00 Hz
.1 Hz	100 Hz "	100.0 Hz
.001 Hz	10 Hz "	10.000 Hz
	100 Hz "	100.000 Hz
	1 kHz "	1000.000 Hz
	10 kHz "	10000.000 Hz
.001 Hz	25 kHz "	0.000 Hz
.001 Hz	1 Hz "	0.000 Hz

should not be illuminated. This checks the out-of-lock feature.

7. Repeat Step 6 for 1 Hz.

8. Set the input signal to 10 Hz. When the display is stable, step the input signal up to 10 kHz. Confirm that the second reading after changing the input signal is correct.

351-18. TROUBLESHOOTING

351-19. If the Resolution Multiplier fails the Performance Check, repair may be necessary. The following steps provide guidelines for troubleshooting.

1. Remove the 7220A top cover.

2. Set the front panel CH A/CH B switch to RES MULT.

3. Apply an appropriate signal between 10 Hz and 10 kHz to the Channel A input.

4. Check the following points using an oscilloscope:

Check:	You should see:
U2-16	+12V
U3-2	Pulses 1000X frequency of input, TTL
U6-12	Pulses 1/10 frequency of U3-2
U5-11	Pulses 1/10 frequency of U6-12
U4-11	Pulses 1/10 frequency of U5-11.

5. Check for pulses at U3-10. The presence of pulses indicates that the phase-locked loop is not locked. Check U2 and the VCO circuit involving Q3 through Q9.

351-20. LIST OF REPLACEABLE PARTS

351-21. A list of replaceable parts for the Resolution Multiplier are provided in Table 351-3. The component locations can be found in Figure 351-3.

Table 351-3. Resolution Multiplier (Option -351)
(See Figure 351-3.)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
C 1, 8		CAP,CER,0.01UF,+80-20%,100V,Z5V	149153	60705	562CZ5UCK101AF1032	2	
C 2- 6, 9		CAP,TA,10UF,+-20%,20V	330662	56289	199D106X0020CA2	6	
C 7		CAP,MICA,22PF,+-5%,500V	148551	09023	CD15CD220J0	1	
CR 1, 2	*	DIODE,SI,BV=75V,IO=150MA,500MW	203323	07910	1N4448	2	
J 6		SOCKET,SINGLE,PWB,FOR 0.025 PIN	375329	00779	85863-3	8	
MP 1		SOCKET,SINGLE,PWB,FOR 0.080 PIN	149112	74970	105-0753	2	
Q 1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	352369	12040	2N4403	1	
Q 2, 10	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	2	
Q 3, 4	*	TRANSISTOR,SI,PNP,HI-SPEED SWITCH	369629	04713	2N5771	2	
Q 5	*	TRANSISTOR,SI,N-JFET,DUAL,TO-71	379271	17856	E421	1	
Q 6	*	TRANSISTOR,SI,P-JFET,TO-92	403600	04713	2N4342	1	
Q 7- 9	*	TRANSISTOR,SI,NPN,HI-SPEED SWITCHING	369645	07263	2N4274	3	
R 1, 3, 24		RES,CF,2.7K,+-5%,0.25W	386490	80031	1-4-5P2K7	3	
R 2, 6, 7,		RES,CF,1K,+-5%,0.25W	343426	59124	CF1-4 102 J B	6	
R 11- 13			343426				
R 4, 20		RES,CF,22K,+-5%,0.25W	348870	59124	CF1-4 223 J B	2	
R 5		RES,CF,560,+-5%,0.25W	385948	80031	5043C225560R0J	1	
R 8, 9		RES,CF,4.7K,+-5%,0.25W	348821	59124	CF1-4 472 J B	2	
R 10, 25		RES,CF,100K,+-5%,0.25W	348920	80031	1-4-5P100K	2	
R 14		RES,CF,3.3K,+-5%,0.25W	348813	80031	1-4-5P3K3	1	
R 15		RES,CF,1.2K,+-5%,0.25W	441378	80031	1-4-5P1K2	1	
R 16, 22		RES,CF,390,+-5%,0.25W	441543	80031	1-4-5P390E	2	
R 17		RES,CF,1M,+-5%,0.25W	348987	80031	1-4-5P1M	1	
R 18		RES,CF,470K,+-5%,0.25W	342634	80031	1-4-5P474K	1	
R 19		RES,CF,150,+-5%,0.25W	343442	59124	CF1-4 151 J B	1	
R 21		RES,CF,820,+-5%,0.25W	442327	80031	1-4-5P820E	1	
R 23		RES,CF,180,+-5%,0.25W	441436	59124	CF1-4 181 J B	1	
R 26		RES,CF,10K,+-5%,0.25W	348839	59124	CF1-4 102 J B	1	
U 2	*	IC,CMOS,PHASE LOCKED LOOP,16 PIN DIP	403584	54590	CD4046BE	1	
U 3	*	IC,TTL,HEX INVERTER W/OPEN COLLECTOR	288605	01295	SN7416N	1	
U 4, 5	*	IC,LSTTL,DIV BY 2,DIV BY 5 COUNTER	402545	01295	SN74LS90N	2	
U 6	*	IC,LSTTL,DIV BY 2,DIV BY 5 PRSET CNTR	393256	01295	SN74LS196N	1	
U 7	*	IC,BPLR,TIMER,8 PIN DIP	402610	18324	NE555N	1	

An * in 'S' column indicates a static-sensitive part.

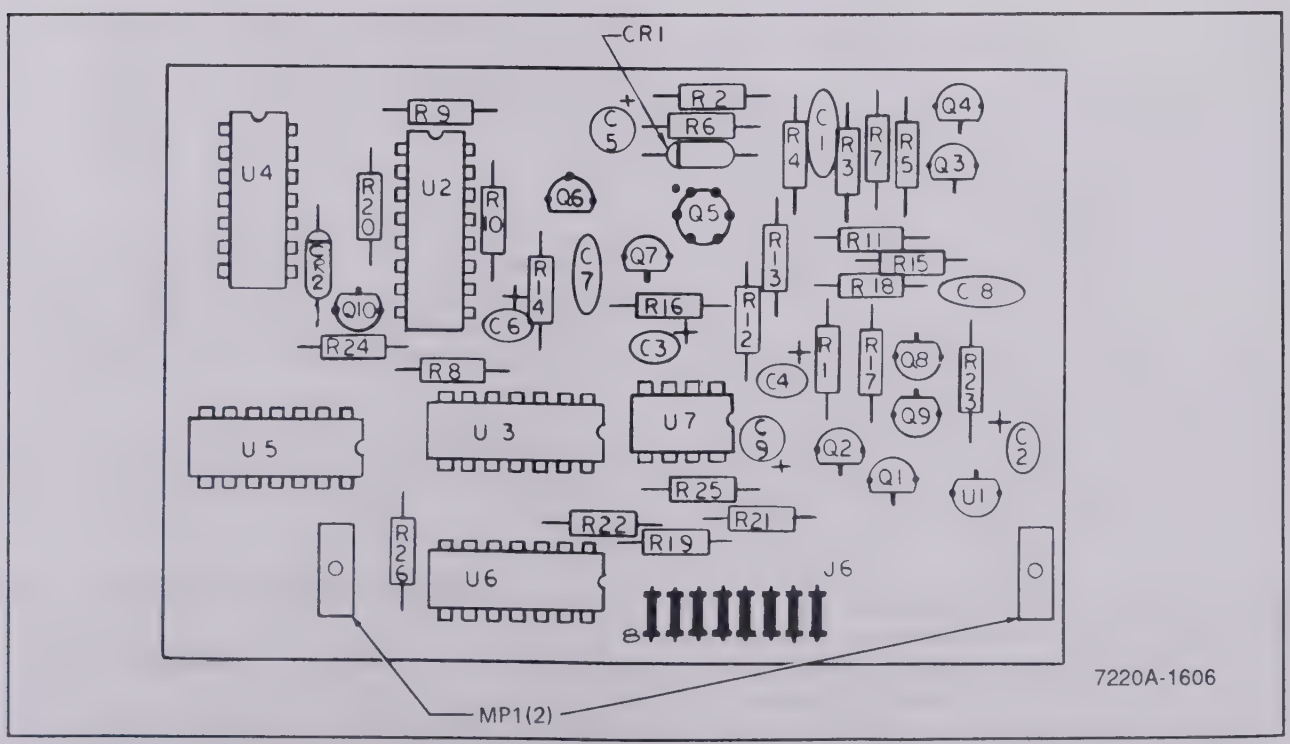


Figure 351-3. Resolution Multiplier (Option -351)

Option -521
Printer Interface

521-1. INTRODUCTION

521-2. The purpose of the Printer Interface is to allow a Fluke counter (7220A, 7250A, 7260A, or 7261A) to be connected to a Fluke printer (2020A, 2021A, or 2030A) for printed output of counter measurements. The Printer Interface consists of the 72XXA-521 Digital Interface PCB, which is factory-installed in the counter.

NOTE

The 72XXA-521 Digital Interface PCB is also used in the IEEE Interface system for the counters. For information about its function in the IEEE Interface, refer to the 72XXA-521/-522 IEEE Interface.

521-3. The 2020A or 2021A printers must have Printer Optioin -004 installed. The 2030A is ready for connection without any additional options. The counter and printer are connected by an accessory cable. The cable is available in either a 2 foot (Y7203), or 5 foot (Y7204) length.

521-4. Data is transferred from the counter to the printer in a bit-parallel, character-serial manner. The printout from the printer includes the measurement reading of the counter and the measurement unit.

521-5. OPERATING INSTRUCTIONS

521-6. Preparation

521-7. To prepare the instruments for printing measurements, follow these steps:

1. Connect the counter and printer together via cable Y7203 or Y7204. Cable connections are made at the rear panel of each instrument.

2. Apply power to each instrument.

3. Apply a valid input signal to the counter, and set the controls as desired.

4. Set the printer controls as desired. If necessary, refer to the printer manual for operating instructions.

521-8. Printing Measurements

521-9. Figure 521-1 shows three examples of measurement printouts made by a 2030A printer. Notice in all 3 examples that all counter digits are printed (either 8 or 9, depending on the counter) including any leading zeros. Notice also in the first example that 8 digits are printed for the 7250A. The 7250A has a 7 digit display, but it supplies 8 digits of valid information to the printer.

521-10. The numbers 2 and 3 in the column at the far left are non-selectable instrument addresses which have been preassigned at the factory in conformance with a printer addressing feature. All the counters have been assigned address 2 except the 7220A, which has been assigned address 3. The 7220A has a unique address because its measurement capacity is one digit greater than the other counters.

521-11. The addresses correspond to a jumper pin on the Digital Interface PCB in the counter. If the printer does not print measurement data correctly, or if it does not print at all, the jumper may be in the wrong position. To check the position or move the jumper, refer to the following paragraph.

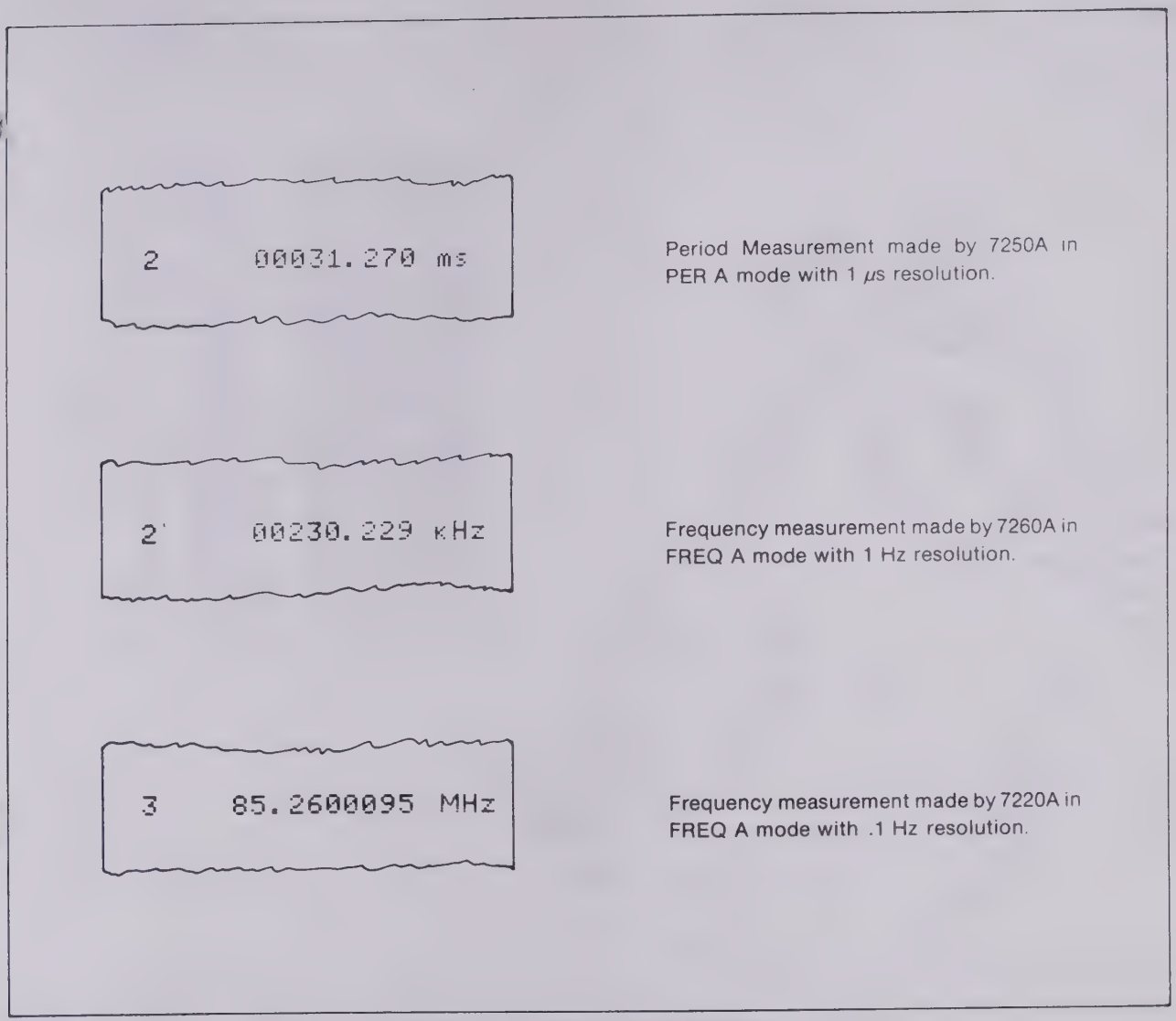

2 00031.270 ms
Period Measurement made by 7250A in PER A mode with 1 μs resolution.
2 00230.229 kHz
Frequency measurement made by 7260A in FREQ A mode with 1 Hz resolution.
3 85.2600095 MHz
Frequency measurement made by 7220A in FREQ A mode with .1 Hz resolution.

Figure 521-1. Printer Output Examples.

521-12. Moving the Address Jumper

WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

521-13. To examine the address jumper, disconnect the counter power cord and remove the top cover of the counter. Be careful not to separate the front and rear panels from the bottom case half. Locate the jumper on the upper left corner of the component side of the Digital Interface PCB. Refer to the table in Figure 521-2, and examine the jumper to determine the address selected. If the proper address is not selected, remove the jumper pin by pulling it straight out. Refer to the table in Figure 521-2 and determine the proper wiper and slot location (the jumper slot numbers are also printed on the back of the PCB). Firmly insert the jumper into place.

521-14. Operating Notes

521-15. In the single print mode, the printer prints the first counter reading it receives and then stops. In the continuous print mode, the printer prints out counter readings as it receives them, up to a maximum rate of 3 readings per second. When the measurement cycle rate of the counter is greater than 3 per second (such as frequency measurements made with 100 Hz resolution), then not all counter readings will be printed out. The printer also will not print out readings made in the Totalize mode by the 7250A, 7260A, or 7261A.

ADDRESS JUMPER

JUMPER POSITION	CONNECTIONS	
	WIPER	SLOT
Do not use 0	W1C	0
Do not use 1	W1A	1
7250A, 7260A, 7261A 2	W1C	2
7220A 3	W1A	3
Do not use 4	W1C	4
Do not use 5	W1B	5
Do not use 6	W1B	6
Do not use 7	W1B	7
Do not use 8	W1A	8
Do not use 9	W1C	9

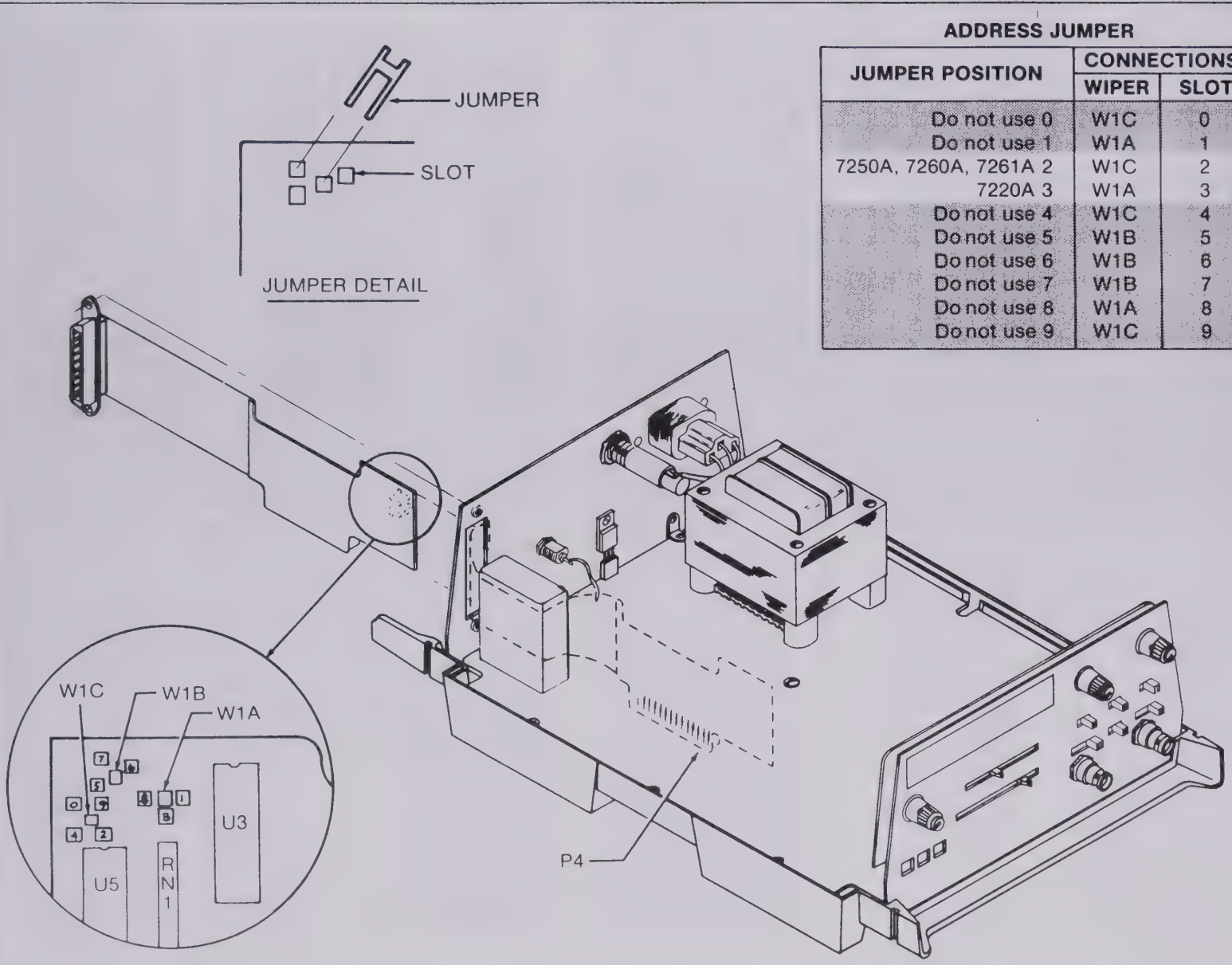


Figure 521-2 Address Jumper

521-16. It is important to note that the printer gives no indication when an overflow condition exists in the counter. The printer will print whatever digits are present in the display at the end of the reading, whether the counter display has overflowed or not. The one exception to this is the 7250A, which supplies eight digits of valid information to the printer before overflowing, even though it has a seven digit display.

521-17. THEORY OF OPERATION

521-18. Overview

521-19. An overview of the operation of the Printer Interface is presented at the top of Figure 521-3. As shown in the figure, the printer functions primarily as a passive listener which receives and prints counter readings without affecting the operation of the counter. The printer does have a limited talk function, however. It must first send an address to the Printer Interface and have the address acknowledged by the Interface before data can be transferred from the counter.

521-20. An expanded view of the interface operation is shown in the large box at the bottom of Figure 521-3. Data transfer is controlled by the control logic, which receives address input from the printer, and three inputs from the counter, OSC, DS1, and BUSY. OSC is the oscillator signal from the scan oscillator that controls the timing of the internal strobing and mutiplexing of the counter. DS1 is the first Digit Strobe (LSD) of the counter, and BUSY is a signal from the control logic of the counter which indicates that a measurement cycle is in progress.

521-21. The Interface Control Logic has three outputs. One output enables the Data Buffer, and the other two are the control lines $\overline{\text{DATVAL}}$ and $\overline{\text{ADRVAL}}$ that are sent to the printer to enable data transfer.

521-22. Detailed Description

521-23. The following paragraphs discuss the sequence of events that take place before, during, and after data transfer. Refer to the block diagram at the bottom of Figure 521-3. The timing can be seen at the top of Figures 521-4 and 521-5, and the circuits are shown in detail in the schematic in Section 8 of the counter Instruction Manual.

521-24. ADDRESS DECODING

521-25. Data Transfer is initiated by the printer. The printer places a 4 bit BCD address on lines A0, A1, A2 and A3. The BCD address is converted to decimal, and if the address corresponds to the address selected by the address jumper, a high signal passes on to the Control Logic. This signal then enables the Data Buffer, and is also inverted and returned to the printer as a low $\overline{\text{ADRVAL}}$.

521-26. DATA TRANSFER

521-27 The low $\overline{\text{ADRVAL}}$ is sent to the microcomputer of the printer and indicates that the Printer Interface has received the address and the counter is preparing to transfer data. After the counter takes a reading, BUSY goes low, then high, which tells the Interface Control Logic a reading has been completed. The next DS1 digit strobe enables the $\overline{\text{DATVAL}}$ line, which is the inverted OSC signal. The digits of the information are now transferred in the sequence indicated in Figures 521-4 and 521-5. The 7220A is shown in a separate figure because it is a nine-digit counter, and nine digits of information are passed instead of eight.

521-28. The timing of the data transfer is controlled by the $\overline{\text{DATVAL}}$ pulses. One $\overline{\text{DATVAL}}$ pulse occurs for each digit of information transferred. All the counters have eight $\overline{\text{DATVAL}}$ pulses except the 7220A, which has nine for its nine digits. The second DS1 digit strobe disables the $\overline{\text{DATVAL}}$ pulses, thus ending the data transfer.

521-29. Data Format

521-30. The format for the data transfer is shown in Figures 521-4 and 521-5. The digits are transferred in the sequence shown, beginning with the LSD, then the MSD, and continuing in descending order of significance. Note that the 7250A provides eight digits of information to the printer even though the 7250A has a seven digit display. The MSD in Figure 521-5 is not displayed on the 7250A, but is printed by the printer. The seven digits displayed on the 7250A are 2SD-LSD.

521-31. There are six lines on which measurement data passes from the counter to the printer. Four of the lines (B1, B2, B4 and B8) transfer the measurement reading in BCD. The DP and UX lines are used to indicate when to insert the decimal point and the type of measurement unit.Table 521-1 shows an example of the format for the transmission of measurement data from a 7250A.

521-32. MAINTENANCE

521-33. Troubleshooting

521-34. If the printer does not print measurment data correctly, or if it does not print at all, first check the position of the address jumper on the Digital Interface PCB. Refer to the section on Moving the Address Jumper in the Operating Instructions.

521-35. If the printer still does not print data correctly, make sure the printer and counter are properly connected with cable Y7203 or Y7204. Apply power to the instruments, select desired settings, and apply a valid input signal to the counter. A non-burst mode must be selected for a 7220A. Use an oscilloscope and complete the procedure given in Table 521-2.

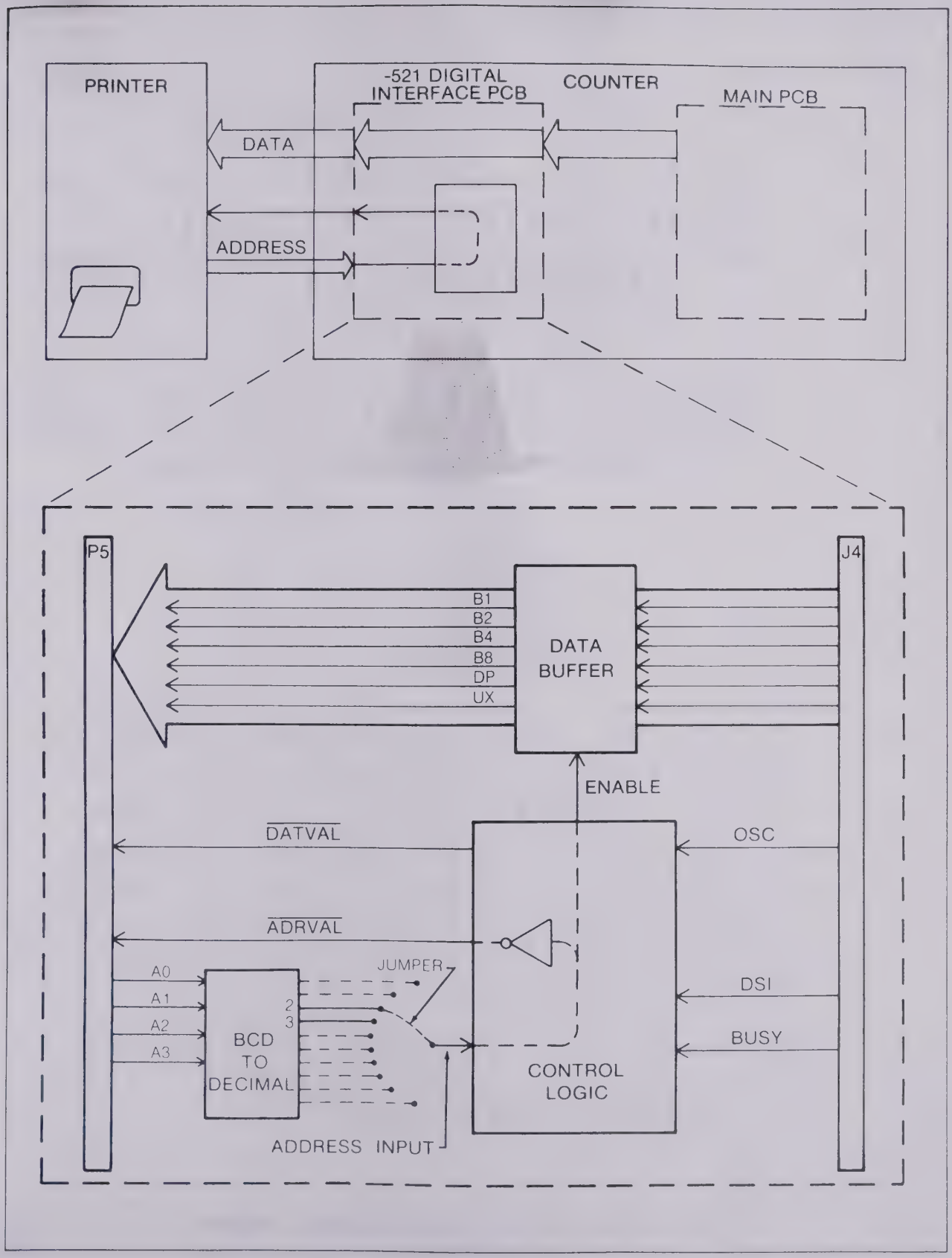
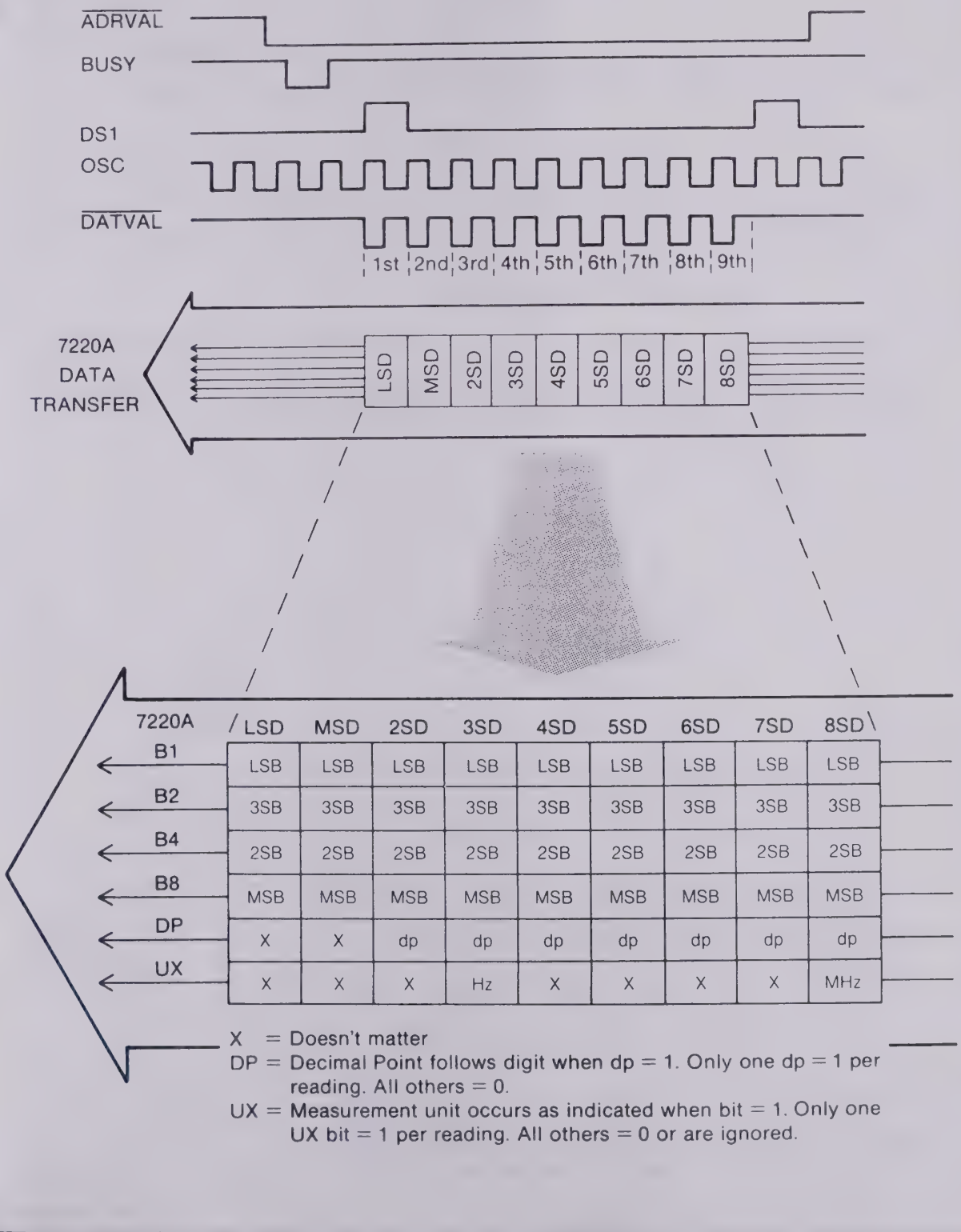


Figure 521-3 Interface Block Diagram


ADRVAL
BUSY
DS1
OSC
DATVAL
1st 2nd 3rd 4th 5th 6th 7th 8th 9th
7220A DATA TRANSFER
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD 8SD
7220A
B1
B2
B4
B8
DP
UX
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD 8SD
LSB LSB LSB LSB LSB LSB LSB LSB LSB
3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB
2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB
MSB MSB MSB MSB MSB MSB MSB MSB MSB
X X dp dp dp dp dp dp dp
X X X Hz X X X X MHz

X = Doesn't matter
DP = Decimal Point follows digit when dp = 1. Only one dp = 1 per reading. All others = 0.
UX = Measurement unit occurs as indicated when bit = 1. Only one UX bit = 1 per reading. All others = 0 or are ignored.

Figure 521-4. 7220A Data Transfer Format and Timing

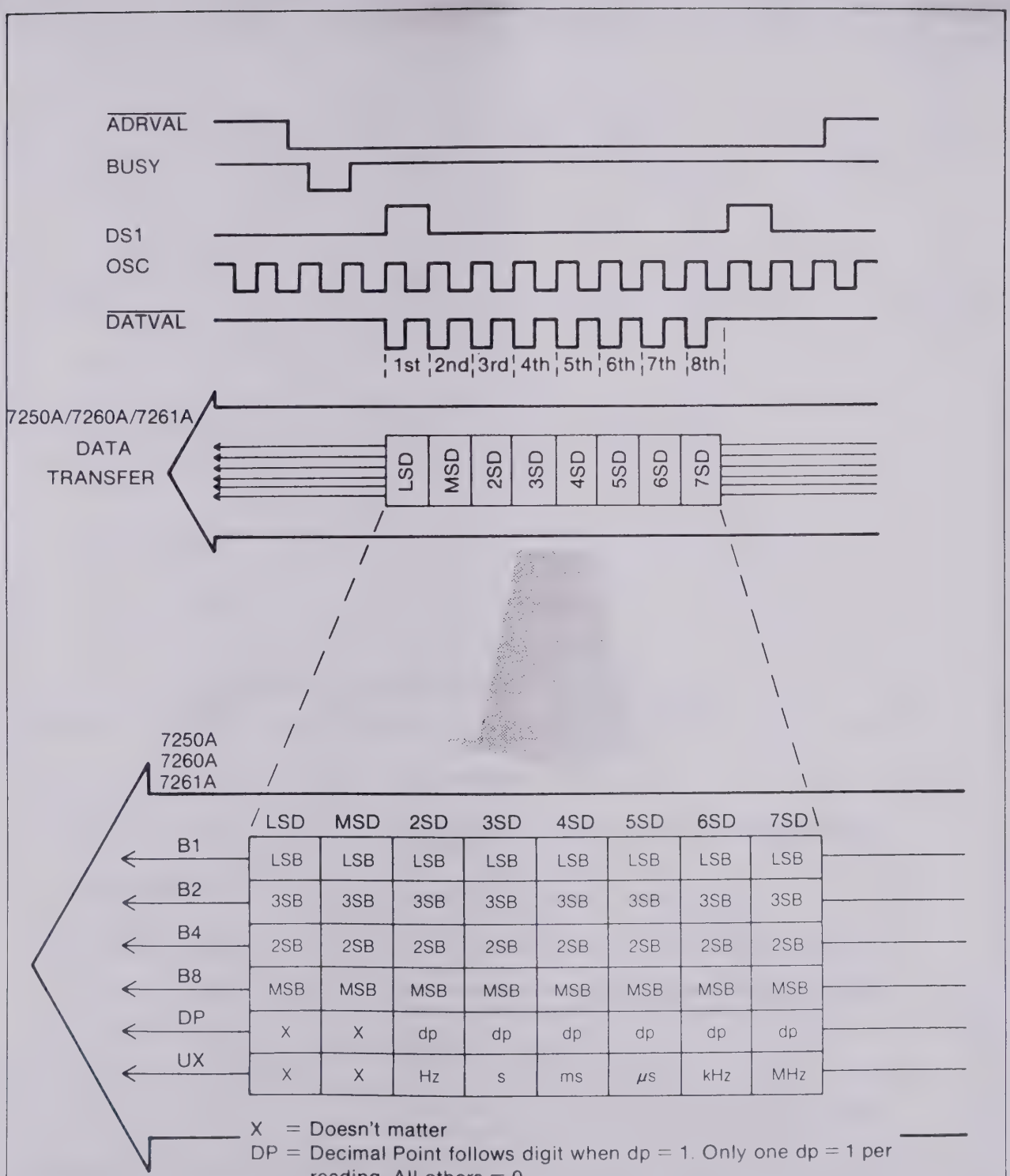

ADRVAL
BUSY
DS1
OSC
DATVAL
1st 2nd 3rd 4th 5th 6th 7th 8th
7250A/7260A/7261A
DATA
TRANSFER
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD
7250A
7260A
7261A
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD
B1 LSB LSB LSB LSB LSB LSB LSB LSB
B2 3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB
B4 2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB
B8 MSB MSB MSB MSB MSB MSB MSB MSB
DP X X dp dp dp dp dp dp
UX X X Hz s ms μs kHz MHz
X = Doesn't matter
DP = Decimal Point follows digit when dp = 1. Only one dp = 1 per reading. All others = 0.
UX = Measurement unit occurs as indicated when bit = 1. Only one UX bit = 1 per reading. All others = 0 or are ignored.

Figure 521-5. 7260A, 7261A, 7250A Data Transfer Format and Timing

Table 521-1. Data Format Example

7250A frequency measurement of 537.387 kHz made in the FREQ A mode with 1 Hz resolution.

	LSD	MSD	2SD	3SD	4SD	5SD	6SD	7SD
B1	1	0	0	1	1	1	1	0
B2	1	0	0	0	1	1	1	0
B4	1	0	0	1	0	1	0	0
B8	0	0	0	0	0	0	0	1
DP	x	x	0	0	0	1	0	0
UX	x	x	0	0	0	0	1	0

x=Doesn't matter

The printer output looks like this:

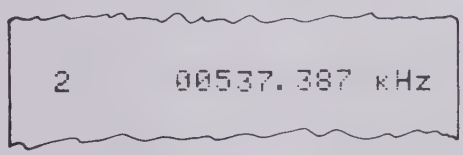


Table 521-2. Troubleshooting Guide-Printer Interface

CHECK:		YOU SHOULD SEE:
Connector J4	Pin 2	+5V (supplied by counter)
Address Decode	U2-5	Positive pulse (CMOS) each time the printer addresses the counter.
U1 Buffer Enable	U3-4	Negative pulse, inverse of pulse on U2-5.
BUSY (BY)	U2-3	Pulses from counter indicating measurement is complete.
	U2-1	Positive pulse, one per print command. Occurs at completion of measurement.
	U2-11	Positive pulses, DSI from display.
	U2-13	Positive pulse, one per print command. Goes high at beginning of DSI, falls at beginning of next DSI.
$\overline{\text{DATVAL}}$	U4-11	Burst of 8 negative pulses (9 for the 7220A), one burst per print command.

521-36. Pin Assignment Table

521-37. Table 521-3 provides a list of the pin assignments for P5, which is the connection at the rear panel of the counter between the Digital Interface PCB and the cable to the printer. For pin assignments for J4, the connection between the Digital Interface PCB and the Main PCB of the counter, see the schematic in Section 8 of the Counter Instruction Manual.

521-38. REPLACEABLE PARTS

521-39. A detailed list of replaceable parts is presented in Table 521-4. Figure 521-6 can be used as an aid in locating components. Refer to Section 5 of the counter instruction manual for parts ordering information.

Table 521-3. P5 Pin Assignments.

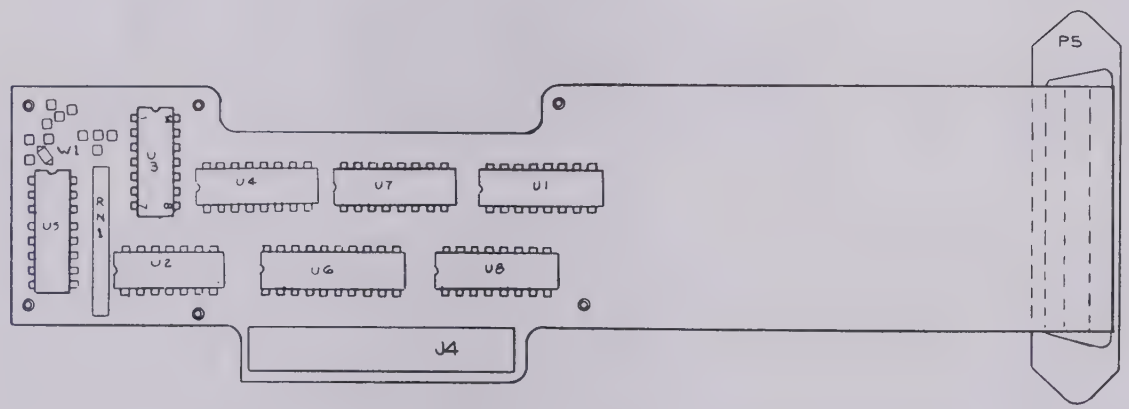
P5 PIN NO.	MNEMONIC	SOURCE		DESCRIPTION
		COUNTER	PRINTER	
1	$\overline{\text{ADRVAL}}$	X		Address Valid
2	$\overline{\text{DATVAL}}$	X		Data Valid
3	A0		X	LSB (Counter Address)
4	A1		X	3SB (Counter Address)
5	A2		X	2SB (Counter Address)
6	A3		X	MSB (Counter Address)
7	not used			
8	not used			
9	D0	X		BCD Bit 1
10	D1	X		BCD Bit 2
11	D2	X		BCD Bit 4
12	D3	X		BCD Bit 8
13	D4	X		Decimal Point (DP)
14	D5	X		Measurement Unit (UX)
15	not used			
16	not used			
17	GND			
18	+5V Supplied by printer			
19-36	not used			

Note: $\overline{\text{BUSEN}}$ (pin no. 22) is always held high when the Printer Interface is used with a printer.

Table 521-4. Digital Interface (Option -521)
(See Figure 521-6.)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOT -E-
H 1		CONN ACC,MICRO-RIBBON,SCREW LOCK KIT	484196	00779	552568-1	2	
J 4		SOCKET,2 ROW,PWB,0.100C,RT ANG 36 POS	484733	00779	4-102084-8	1	
MP 1		INSULATOR, GUARD COVER	492298	89536	492298	1	
P 5		CONN, MODIFIED, MICRO RIBBON, REC	479493	89536	479493	1	
RN 1		RES,CERM,SIP,10 PIN,9 RES,100K,+-2%	544247	91637	CSC10A-01-104-G	1	
U 1, 7, 8	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	04713	MC14503BCP	3	
U 2	*	IC,CMOS,DUAL D F/F,+EDG TRIG	340117	04713	MC14013CL	1	
U 3	*	IC,CMOS,QUAD 2 INPUT NAND GATE	355198	04713	MC14011UBCP	1	
U 4	*	IC,LSTTL,HEX BUFFER W/NOR ENABLE	483800	01295	SN74LS367AN	1	
U 5	*	IC,CMOS,BCD-DECIMAL DECODER	380741	01295	TP4028AN	1	
U 6	*	IC,LSTTL,OCTL BUFFER W/3-ST&NOR ENABL	429902	27014	DM81LS95AN	1	
W 1		JUMPER,DIP,0.100CTR	416842	91506	8136-651P2	1	
XW 1		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	

An * in 'S' column indicates a static-sensitive part.



7220A-1607

Figure 521-6. Digital Interface (Option -521)

Section 7
Schematic Diagrams

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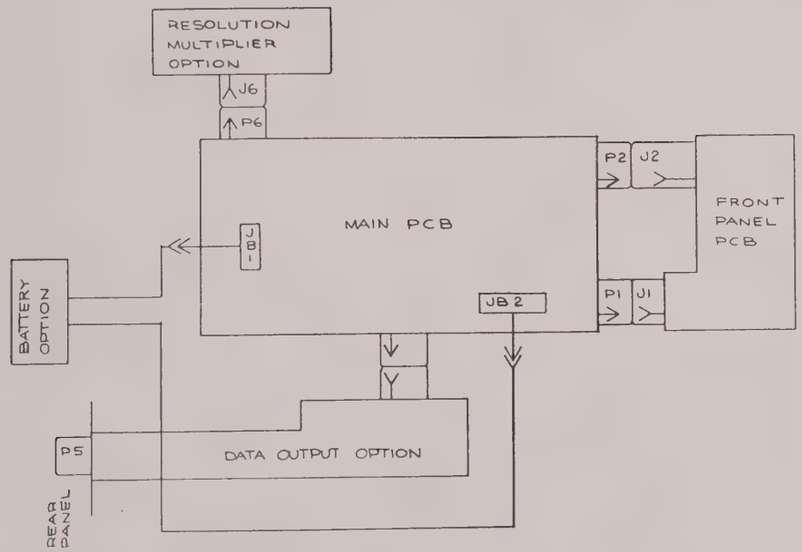
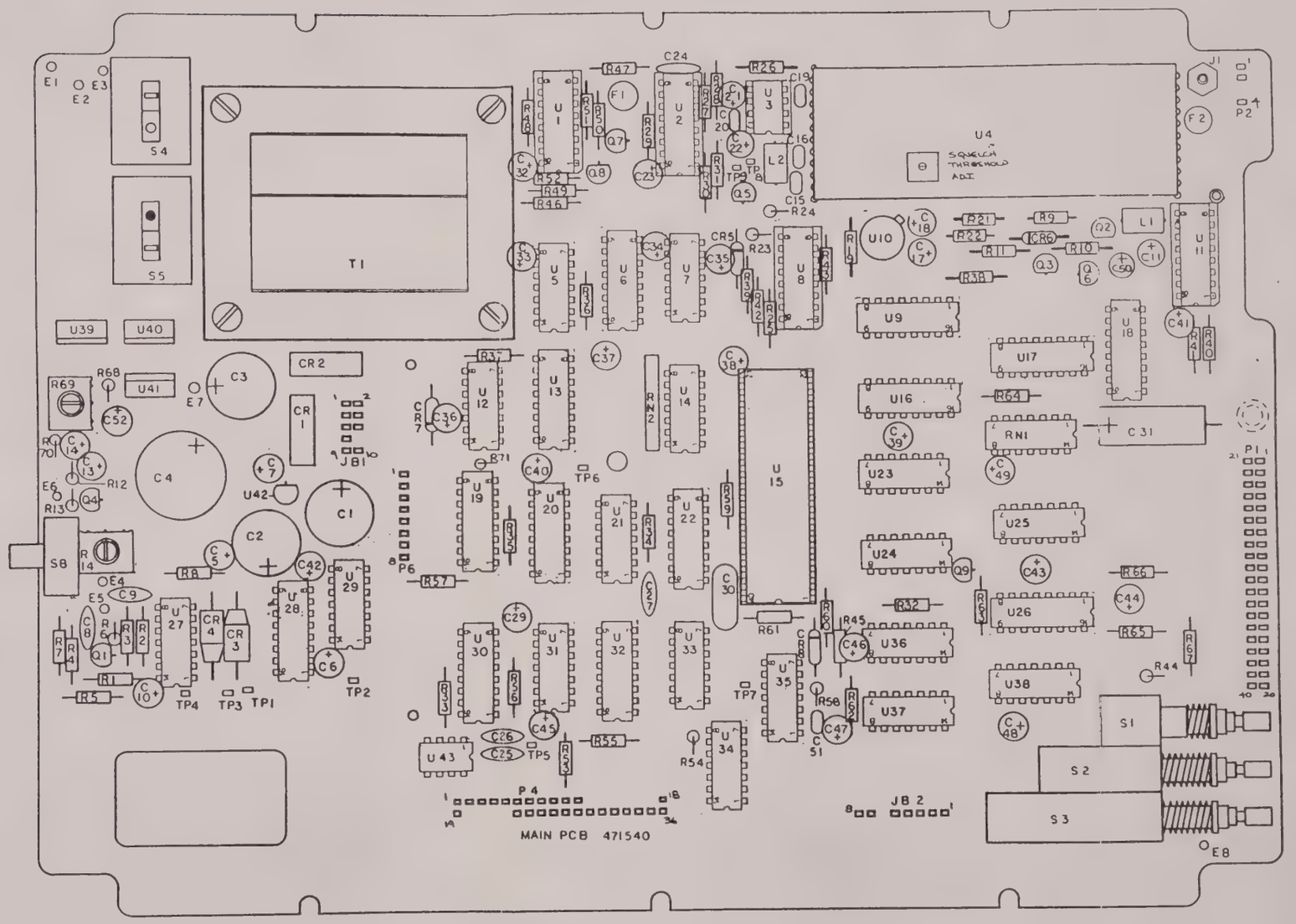
MNEMONICS

a, b, c, d, e, f, g	7 segment LED display information.
$\overline{\text{ADRVAL}}$	Address Valid. Printer interface signal.
AECL	Channel A Emitter-Coupled Logic.
ATTL	Channel A Transistor-Transistor Logic.
$\overline{\text{ATN}}$	Attention. IEEE Bus management line.
B1, B2, B4, B8	Binary coded decimal measurement bits from multiplexer to Digital Interface.
B1D1, B2D1, B3D1, B4D1	Binary coded decimal bits for digit 1.
B1D2, B2D2, B3D2, B4D2	Binary coded decimal bits for digit 2.
$\overline{\text{BE}}$	Channel B Enable.
$\overline{\text{BECL}}$	Channel B Emitter-Coupled Logic.
BST	BURST mode selected.
$\overline{\text{BUSEN}}$	Bus Enable.
BUSY, BY	Busy signal from Control Logic when measurement cycle is in progress.
CH A	Channel A mode selected.
CH B	Channel B mode selected.
CHK	Self-check mode selected.
D1, D2, D3, D4	Binary coded decimal measurement bits.
$\overline{\text{D1 01}}$ through $\overline{\text{D1 08}}$	IEEE data lines.
DAC	Data Accepted.
$\overline{\text{DAV}}$	Data Valid. IEEE handshake line.
$\overline{\text{DATVAL}}$	Data Valid. Printer Interface signal.
DP	Decimal Point.
DP1, DP2, DP3, DP4	Decimal point display position.
DET OUT	Detector Out from hybrid.
DET REF	Detector Reference from hybrid.
DS1 through DS8	Digit Strobe 1 through Digit Strobe 8.
$\overline{\text{EOI}}$	End or Identify. IEEE Bus management line.
FM	Frequency Multiplier. Channel A conditioned input signal multiplied by 1000.
$\overline{\text{GQ}}$	Main Gate FF $\overline{Q}$ output.
$\overline{\text{GATE}}$	Gate indication to front panel LED display.
HOLD	Single or Continuous measurement selection.
$\overline{\text{IFC}}$	Interface Clear. IEEE Bus management line.
$\overline{\text{LISTEN}}$	IEEE Interface Listen status.
$\overline{\text{M}}$	Measurement Update.
MULT	Resolution Multiplier mode selected.
$\overline{\text{MULT}}$	Non-Resolution Multiplier mode selected.
$\overline{\text{NDAC}}$	Not Data Accepted.
$\overline{\text{NRFD}}$	Not Ready For Data
R, $\overline{\text{R}}$	Reset from Control Logic. Resets latches and accumulators.
$\overline{\text{R'}}$	Reset from Control Logic. Resets Channel B Squelch Latch.
$\overline{\text{REM}}$, $\overline{\text{REN}}$	Remote Enable.
RESET, $\overline{\text{RESET}}$	Front panel Reset.
$\overline{\text{RESETM}}$	Channel A Frequency Multiplier Reset.
RFD	Ready For Data.
$\overline{\text{RNG1}}$, $\overline{\text{RNG2}}$	Resolution Range lines.
S1 through S9	Digit Strobe 1 through Digit Strobe 9.
SC	Single or Continuous measurement selection.
$\overline{\text{SRQ}}$	Service Request.
ST, START	Remote Reset.
$\overline{\text{TALK}}$	IEEE Interface Talk status.
$\overline{\text{TALKEN}}$	IEEE Interface Talk Enable.
UX	Display Annunciator.



7220A-1301

Figure 7-1. Interconnect Diagram

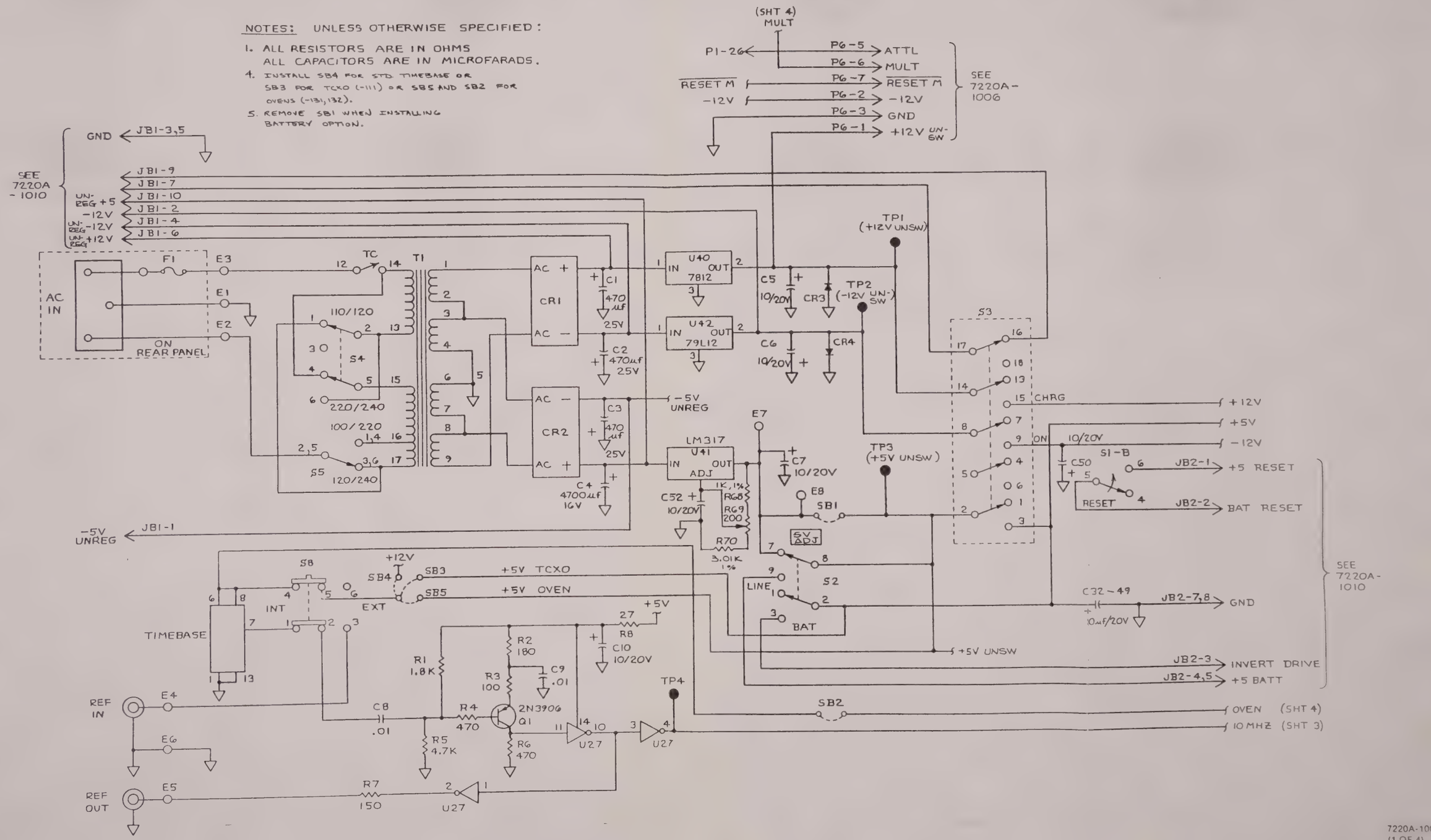


7220A-1601

Figure 7-2. A1 Main PCB Assembly

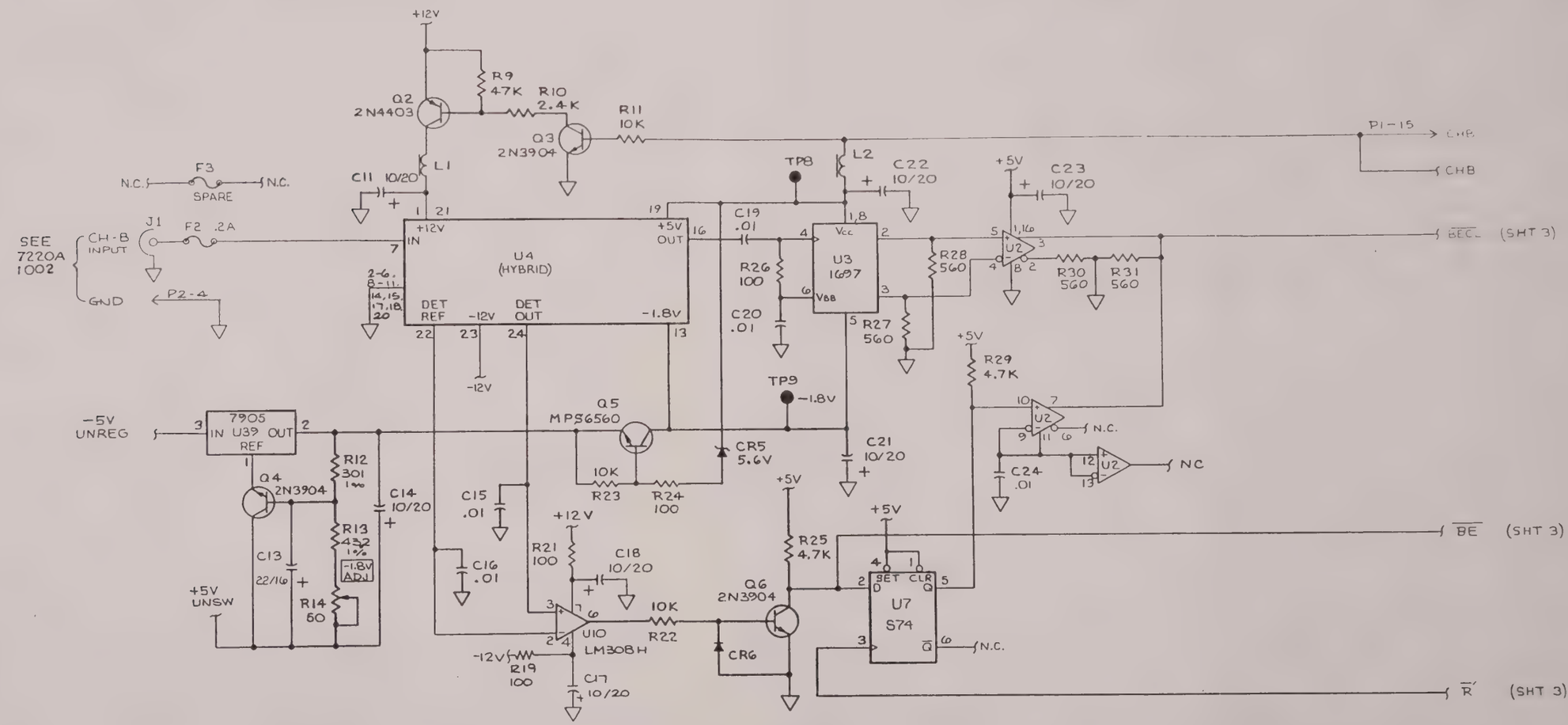
NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS
   ALL CAPACITORS ARE IN MICROFARADS.
4. INSTALL SB4 FOR STD. TIMEBASE OR SB3 FOR TCXO (-111) OR SB5 AND SB2 FOR OVENS (-131,132).
5. REMOVE SB1 WHEN INSTALLING BATTERY OPTION.



7220A-100
(1 OF 4)

Figure 7-2. A1 Main PCB Assembly (cont)



REF DES	+5V	GND	+12	-12
U1	1,16	8		
U2,11	1,16	8		
U3	—	—		
U5	14	7		
U6,13	16	8		
U7	14	7		
U8	1,16	8		
U9	16	8		
U10	—	—		
U12	14	7		
U14,23	5	10		
U15	27	23		26
U16	16	8		
U17	16	8		
U18,22	1	8		
U19	16	8		
U20	15	2		16
U21	14	7		
U24	14	7		
U25,36	11	4		
U26	16	8		
U27	14	7		
U28	16	8		
U29	14	7		
U30	1	8		
U31	14	7		
U32	16	8		
U33	14	7		
U34,35	14	7		
U37,38	14	7		
U39				
U40		3		
U41		3		
U42		1		
U43	4,8	1		

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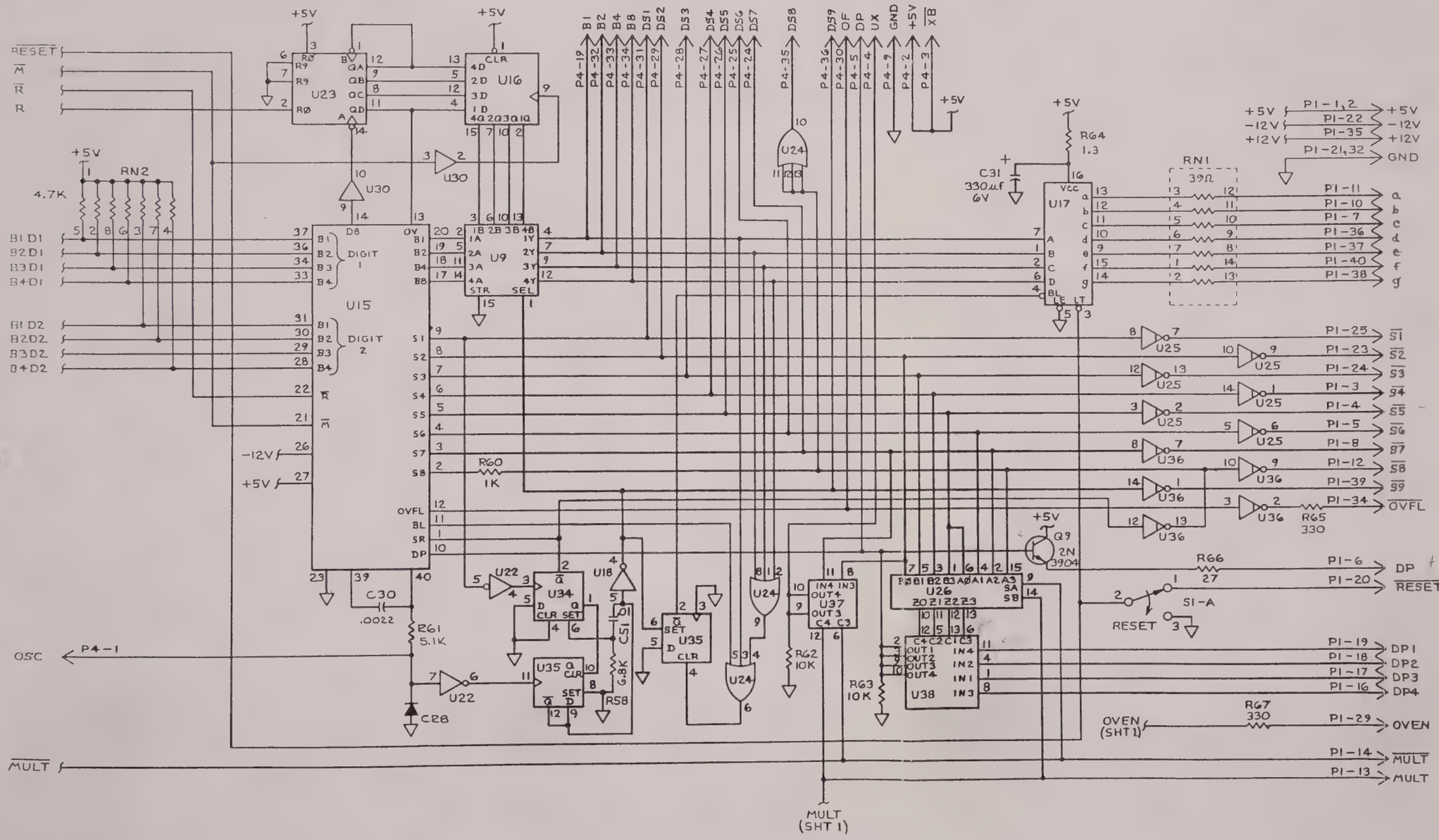
(2 OF 4)

Figure 7-2. A1 Main PCB Assembly (cont)

REF DES	+5V	GND	+12	-12
U1	1,16	8		
U2,11	1,16	8		
U3	—	—		
U5	14	7		
U6,13	16	8		
U7	14	7		
U8	1,16	8		
U9	16	8		
U10	—	—		
U12	14	7		
U14,23	5	10		
U15	27	23		16
U16	16	8		
U17	16	8		
U18,22	1	8		
U19	16	8		
U20	15	2		16
U21	14	7		
U24	14	7		
U25,36	11	4		
U26	16	8		
U27	14	7		
U28	16	8		
U29	14	7		
U30	1	8		
U31	14	7		
U32	16	8		
U33	14	7		
U34,35	14	7		
U37,38	14	7		
U39				
U40		3		
U41		3		
U42		1		
U43	4,8	1		

7220A-1001
(3 OF 4)

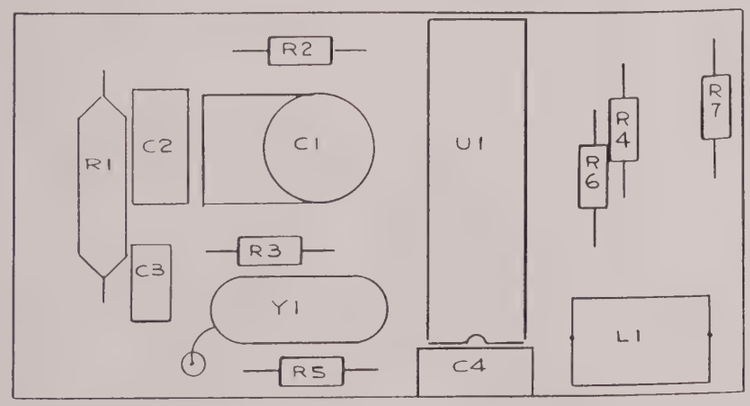
Figure 7-2. A1 Main PCB Assembly (cont)

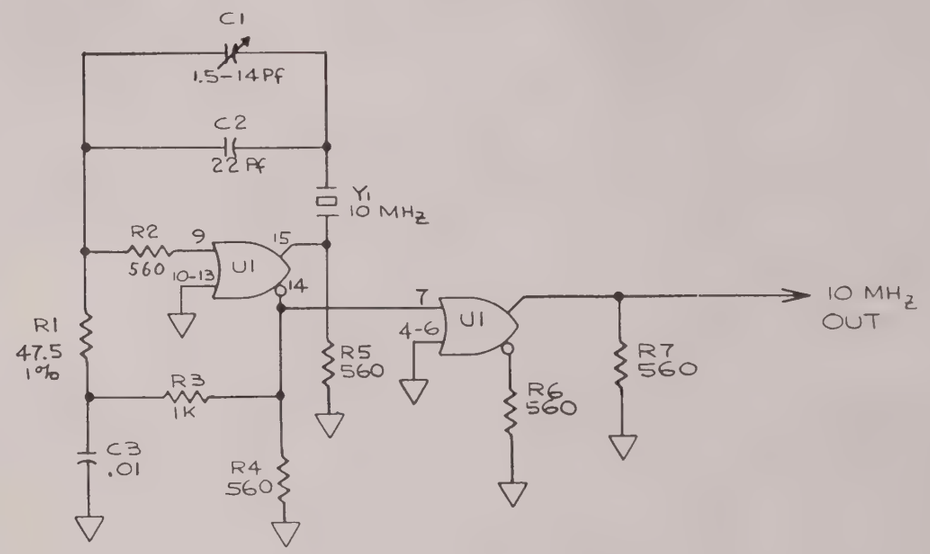


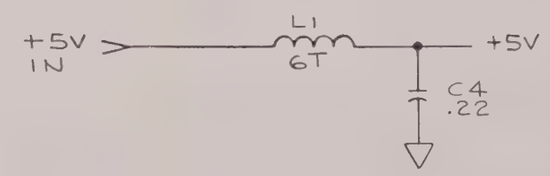
REF DES	+5V	GND	+12	-12
U1	1,16	8		
U2,11	1,16	8		
U3	—	—		
U5	14	7		
U6,13	16	8		
U7	14	7		
U8	1,16	8		
U9	16	8		
U10	—	—		
U12	14	7		
U14,23	5	10		
U15	27	23		26
U16	16	8		
U17	16	8		
U18,22	1	8		
U19	16	8		
U20	15	2		16
U21	14	7		
U24	14	7		
U25,36	11	4		
U26	16	8		
U27	14	7		
U28	16	8		
U29	14	7		
U30	1	8		
U31	14	7		
U32	16	8		
U33	14	7		
U34,35	14	7		
U37,38	14	7		
U39				
U40		3		
U41		3		
U42		1		
U43	4,8	1		

7220A-1001
(4 OF 4)

Figure 7-2. A1 Main PCB Assembly (cont)







NOTES :

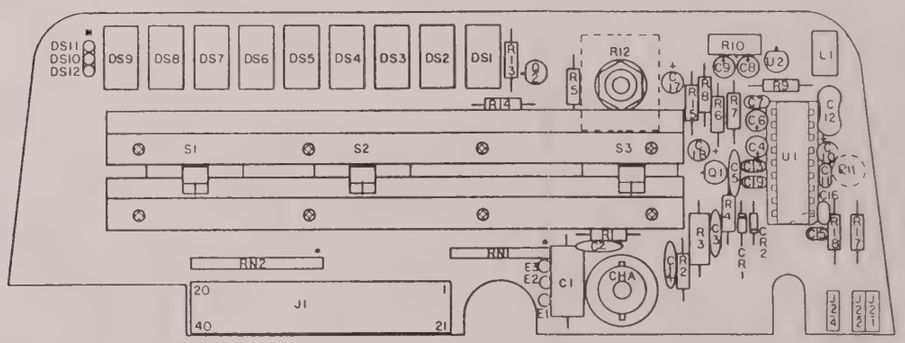
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/8W.
   ALL CAPACITORS ARE IN MICROFARADS

QTY	DEVICE	+5V	GND	REF DES
1	MC10109	1,16	8	U1

7220A-1609

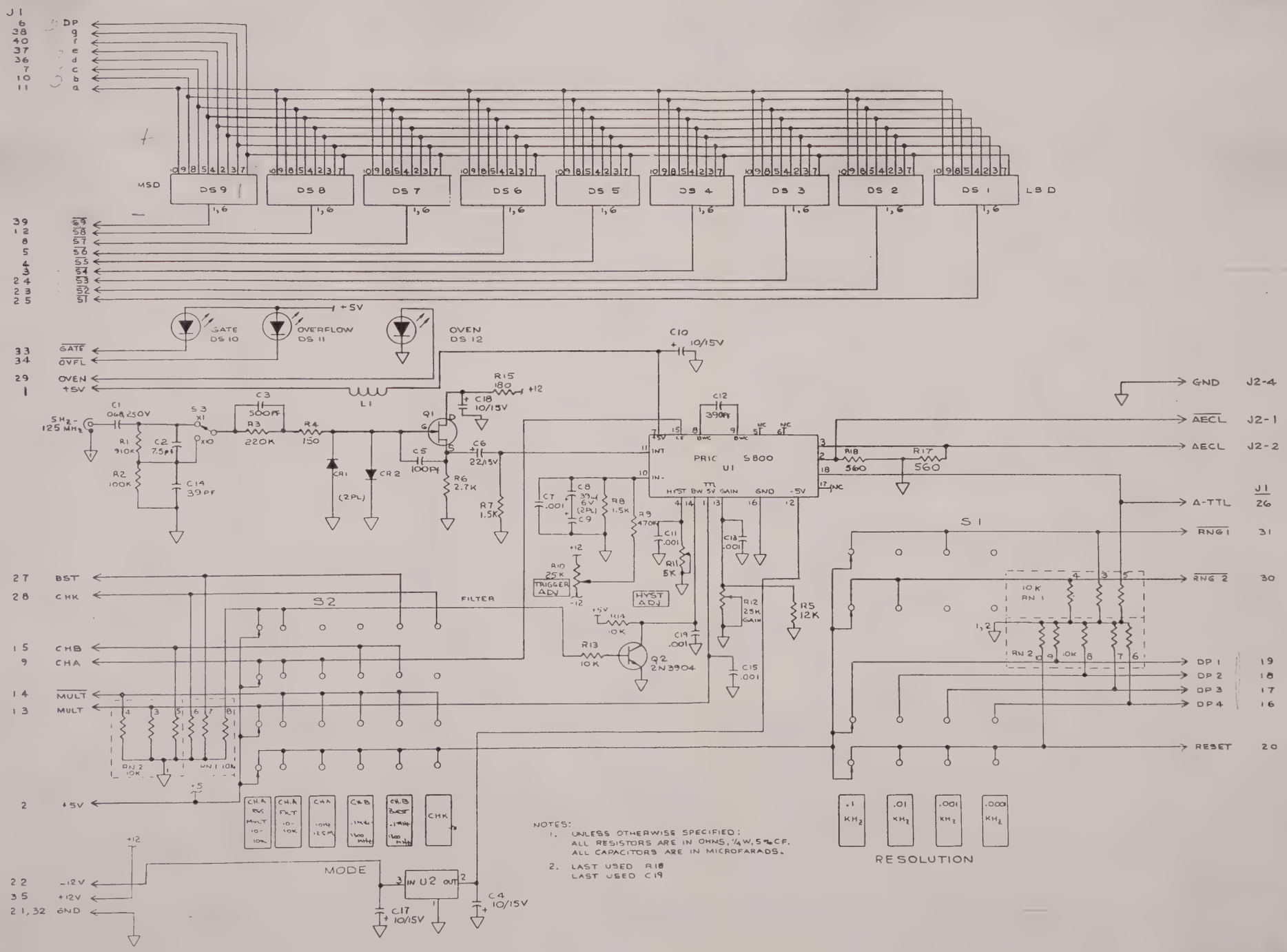
7220A-1009

Figure 7-3. A3 Timebase PCB Assembly



7220A-1602

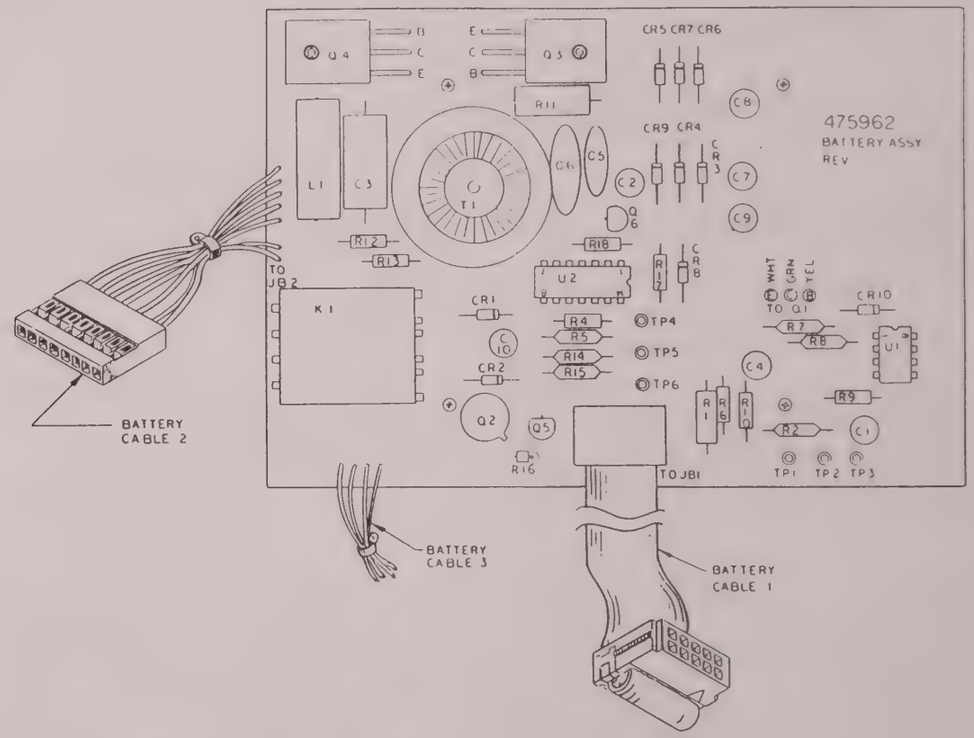
Figure 7-4. A2 Front Panel PCB Assembly



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/4W, 5% CF.
   ALL CAPACITORS ARE IN MICROFARADS.
2. LAST USED R18
   LAST USED C19

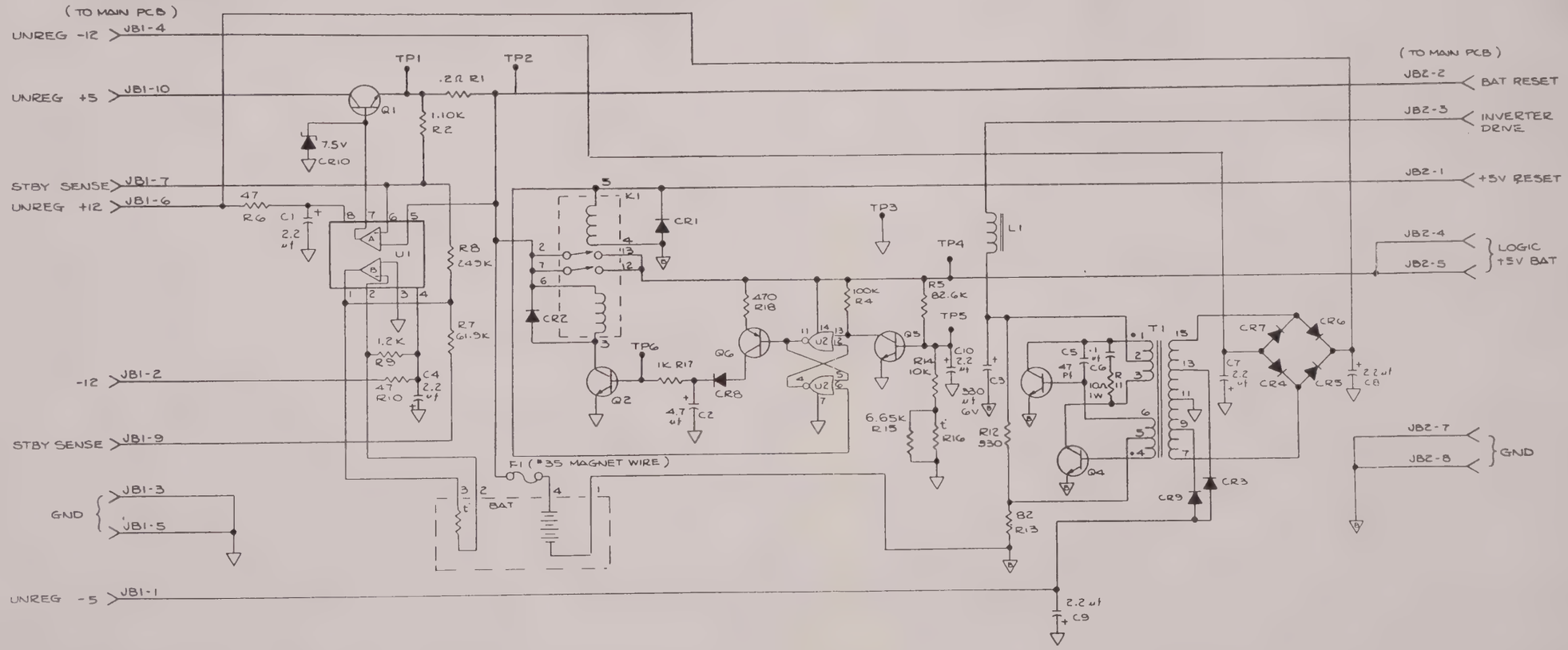
7220A-1002

Figure 7-4. A2 Front Panel PCB Assembly (cont)



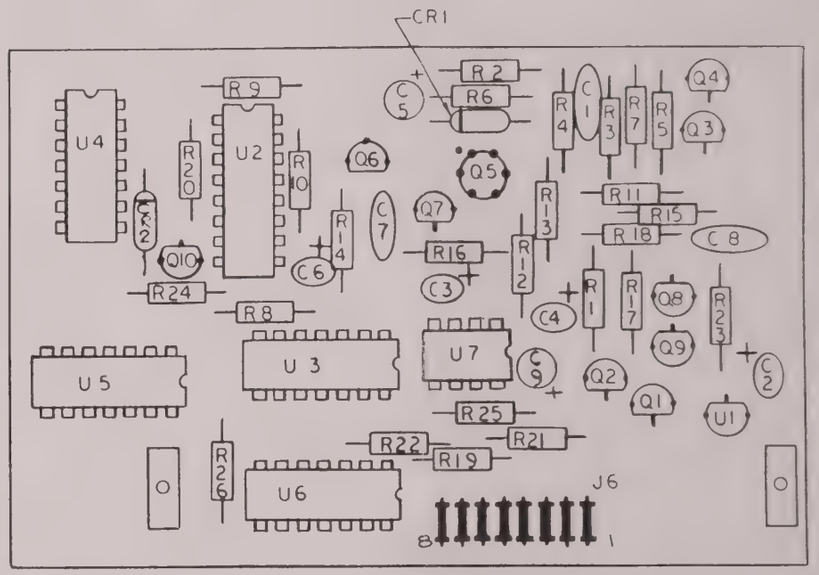
7220A-1610

Figure 7-5. Battery PCB Assembly Option -010



7220A-1010

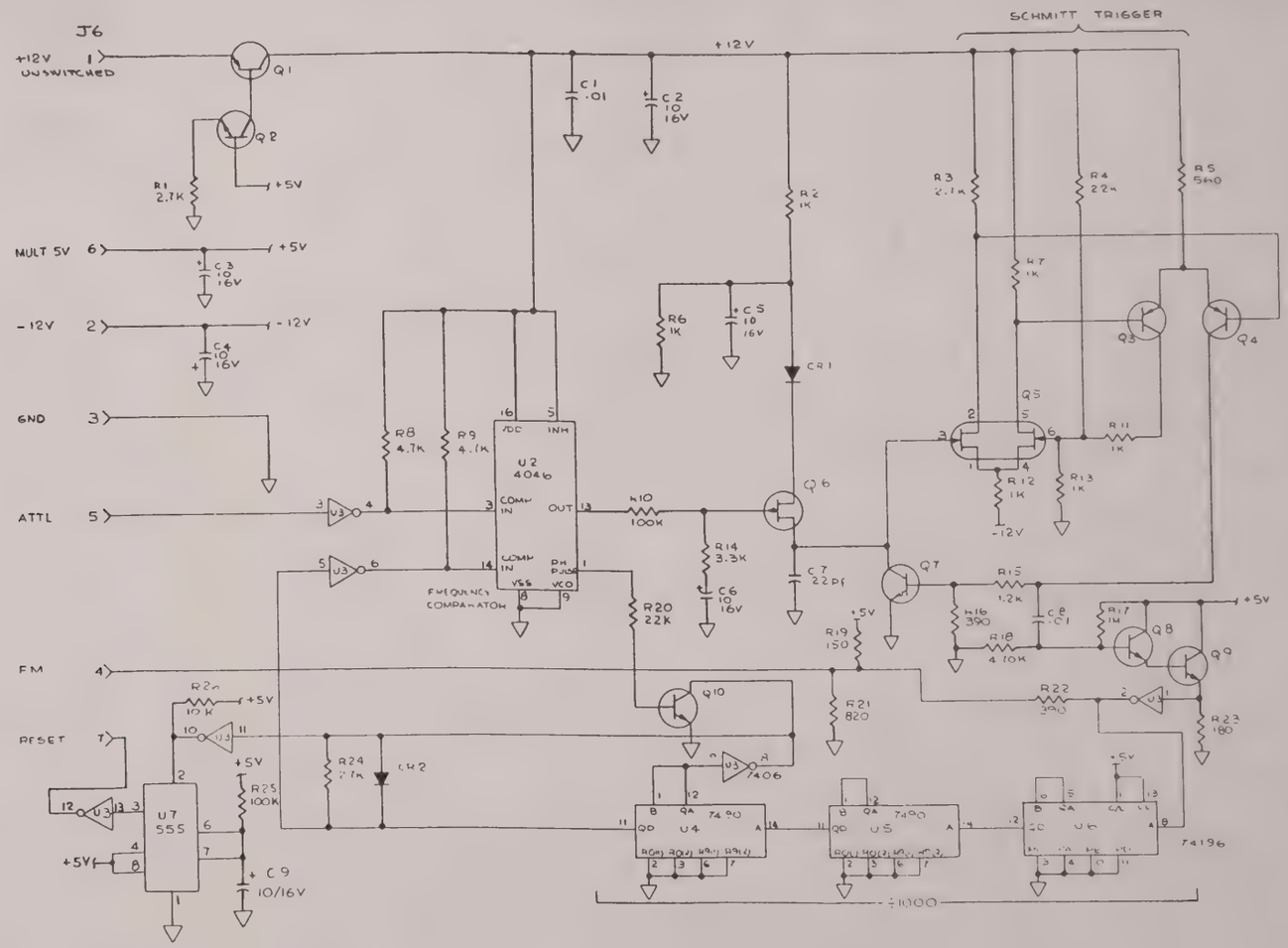
Figure 7-5. Battery PCB Assembly Option -010 (cont)



7220A-1606

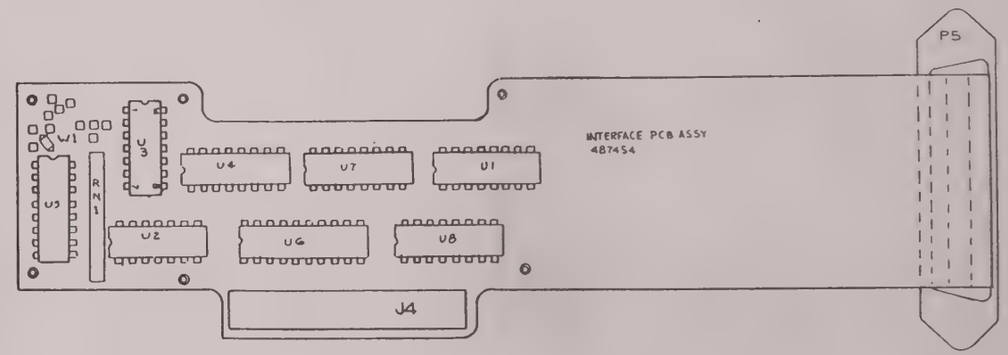
Figure 7-6. Resolution Multiplier PCB Assembly Option -351

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/4W, 5% CC.
   ALL CAPACITORS ARE IN MICROFARADS.



7220A-1006

Figure 7-6. Resolution Multiplier PCB Assembly Option -351 (cont)



7220A-1607

Figure 7-7. Digital Interface PCB Assembly Option -521

P5 INTERFACE CONNECTOR

9 D1
10 D2
11 D3
12 D4
13 DP
14 UX
22 BUSEN
3 F2
4 F8
5 F1
6 HOLD
17 GND
2 A+
1 B+
27 BUSY

P5

23 XB
19 REM
24 GATE
25 START
7 F4
18 R1
16 R2
15 R4
35 RESET
8 FILTER
30 S7
20 S6
21 S5
34 S4
32 S3
33 OVRFLW
28 S0
36 S9
29 S1
31 S2

TO MAIN PCB

J4

B1 19
B2 32
B4 33
B8 34
DP 5
UX 4
+5V 2
GND 9
F2R 13
F8R 12
F1R 15
SCR 10
BY 8
5LB+R 21
5LA+R 22
OSC 1
XB 3
REM 6
GOR 7
STR 11
F4R 14
R1R 16
R2R 17
R4R 18
RSTR 20
FILTR 23
DS7 24
DS6 25
DS5 26
DS4 27
DS3 28
OF 30
DS0 35
DS9 36
DS1 31
DS2 29

RN1 100K

4028 U5

W1 ADDRESS SELECT JUMPER

U2 4013

100K (RN1)

NOTES: UNLESS OTHERWISE SPECIFIED

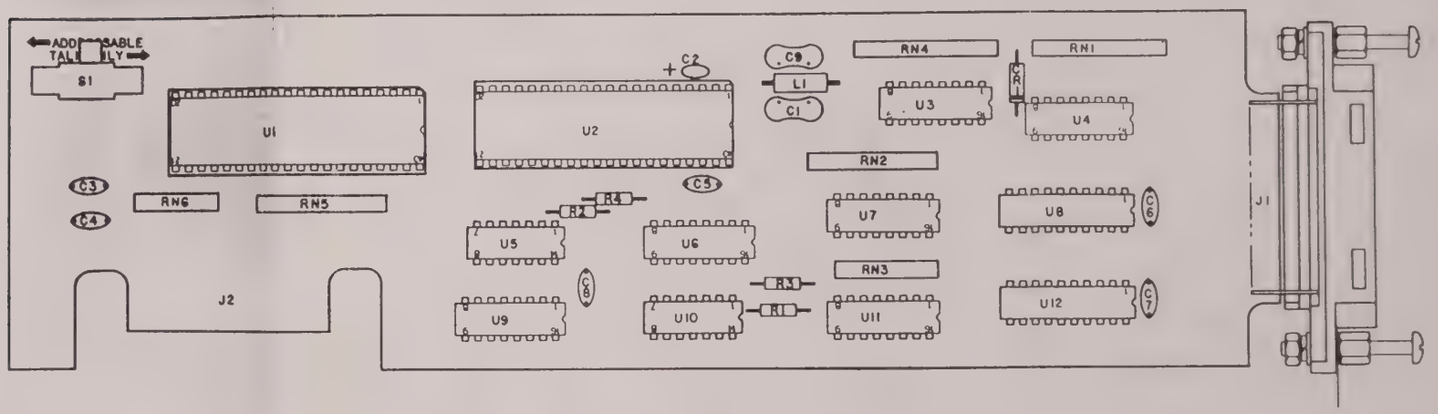
1. ALL RESISTORS ARE IN OHMS

4. POWER CONNECTIONS:

REF DES	TYPE (REF)	GND	+5V
U1	40097	8	16
U2	4013	7, 8	5, 14
U3	4011	7	14
U4	74LS367	8	16
U5	4028	8	16
U6	81LS95	10, 8	20

7220A-1007

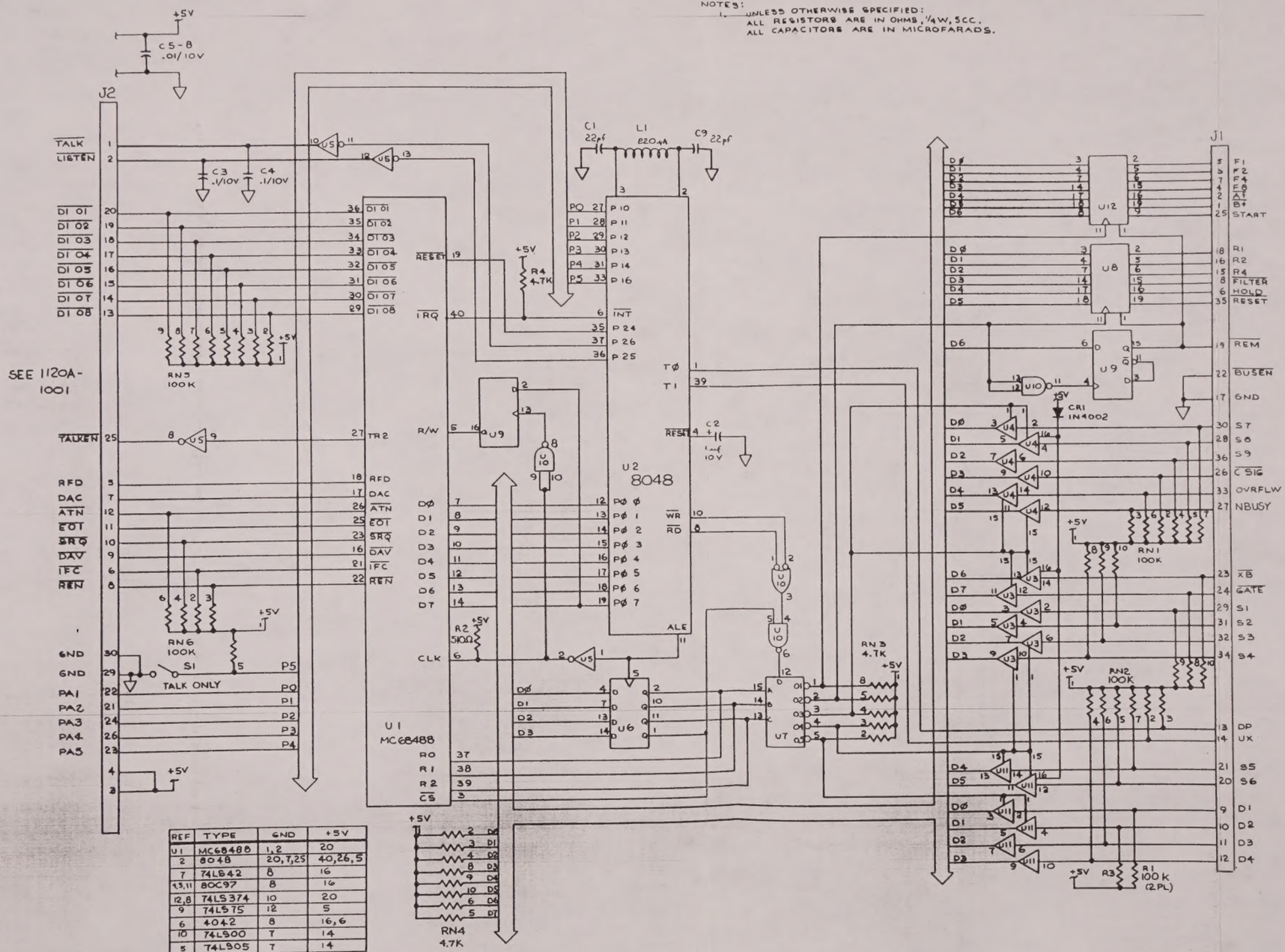
Figure 7-7. Digital Interface PCB Assembly Option -521 (cont)



1120A-1604

Figure 7-8. Interface PCB Assembly Option -522

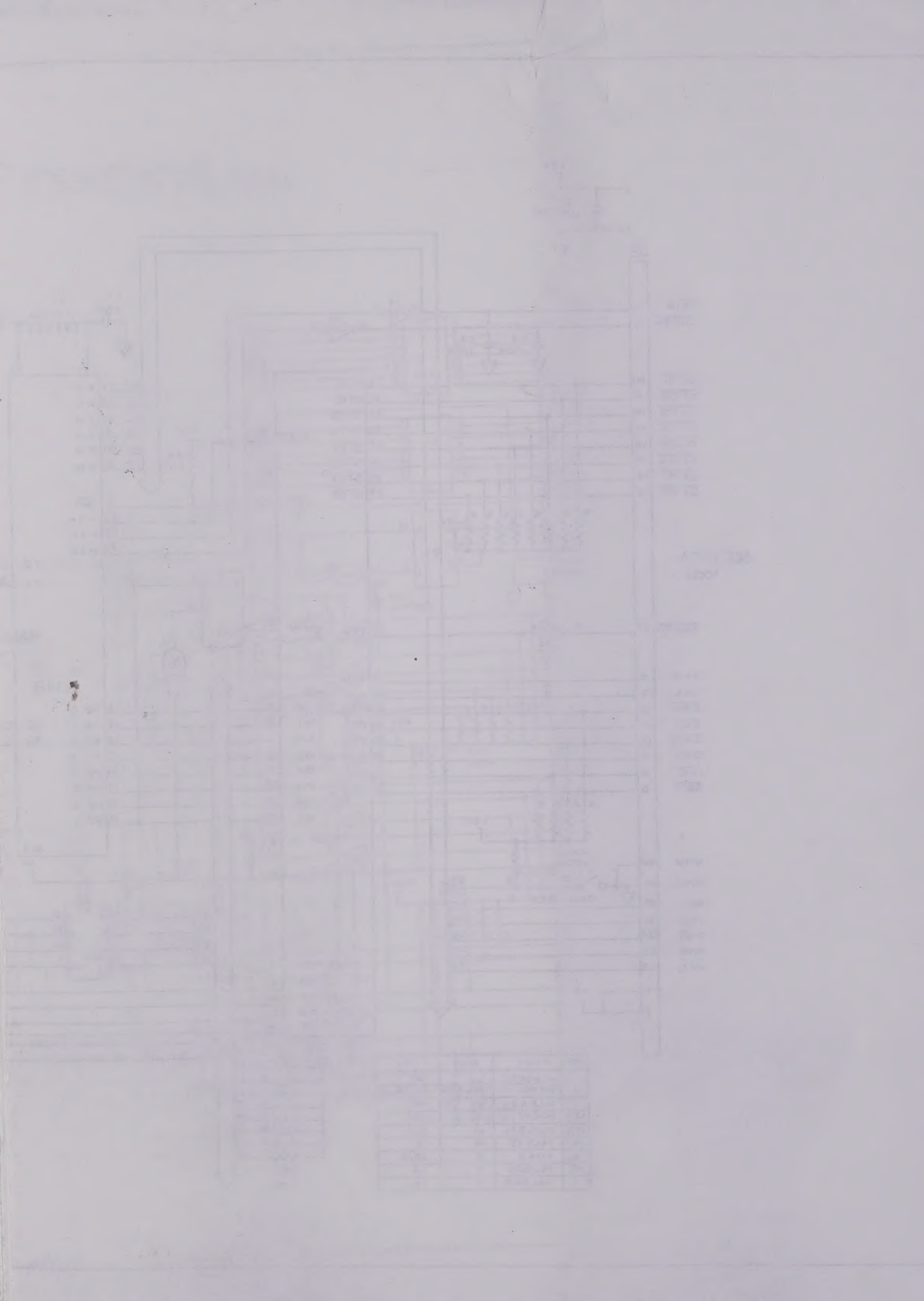
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/4W, 5CC.
   ALL CAPACITORS ARE IN MICROFARADS.



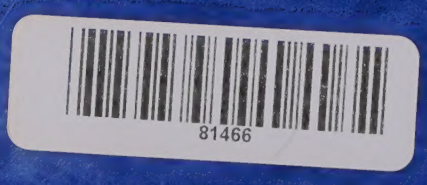
REF	TYPE	GND	+5V
U1	MC68488	1,2	20
2	8048	20,7,25	40,26,5
7	74LS42	8	16
1,3,11	80C97	8	16
12,8	74LS374	10	20
9	74LS75	12	5
6	4042	8	16,6
10	74LS00	7	14
5	74LS05	7	14

1120A-1004

Figure 7-8. Interface PCB Assembly Option -522 (cont)



ACCO® USA
WHEELING, ILLINOIS 60090
25973
MADE IN USA
0 50505 25973 1
DK.BLUE/RL.BLEU/AZUL OBSCURO


81466